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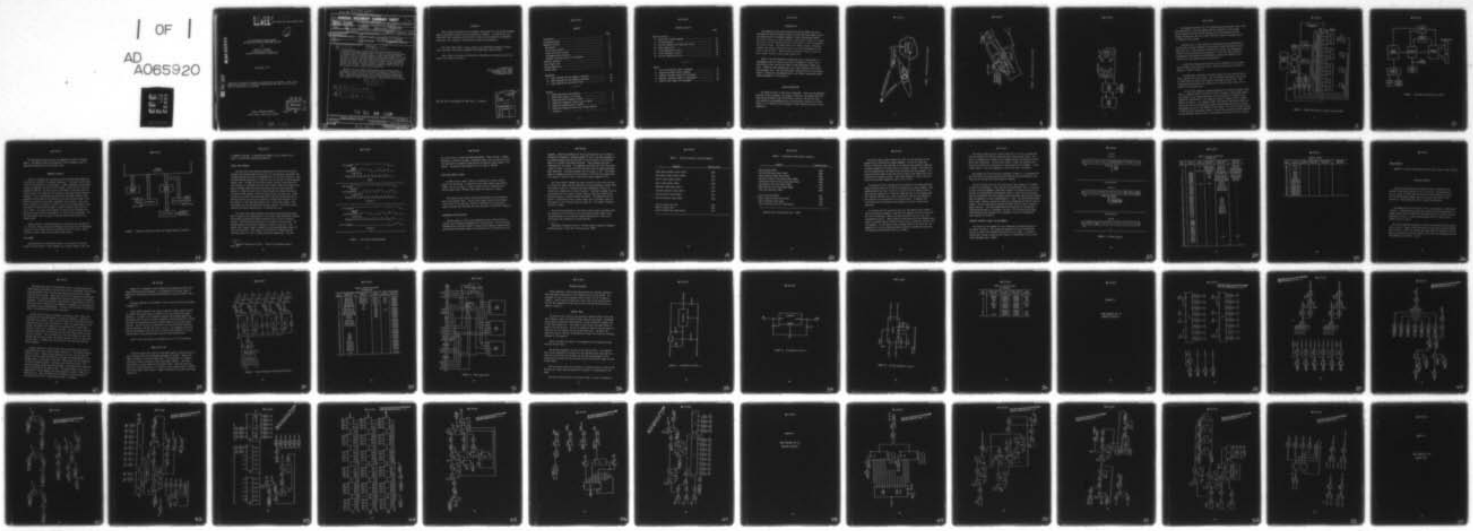

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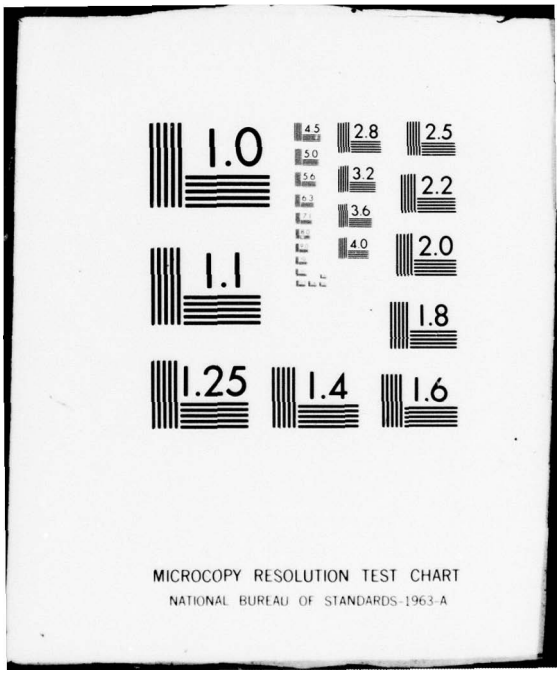
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NWC Technical Memorandum 2475

NWC ADVANCED VISUAL TARGET ACQUISITION SYSTEM HARDWARE DESIGN

by

Neil R. Krenzel
Assessment Division
Systems Development Department

September 1975

NAVAL WEAPONS CENTER
China Lake, California 93555

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The Advanced Visual Target Acquisition System (AVTAS) has been developed by the Naval Weapons Center to enable the Agile weapon system to rapidly acquire an airborne target at large off-boresight angles. The pilot's task is to simply establish a good sight picture of a target and line up on that target an optical sight which is rigidly attached to the pilot's helmet. The AVTAS, which is a helmet tracker, ultimately computes the digital direction cosines in aircraft coordination of the pilot's line of sight. These direction cosines are used to drive the Agile seeker system to rapid target acquisition.

AVTAS is an electro-optical system that uses no moving parts, is lightweight, does not restrict the pilot's movement or vision, has a wide field of view, and can be flown in high performance fighter aircraft. AVTAS has been designed for use in both laboratory and flight test programs to evaluate the operational characteristics of the system.

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FOREWORD

This report describes the hardware developed for the Naval Weapons Center Advanced Visual Target Acquisition System. Included are the detailed logic drawings and specific data with sequential procedures necessary for computer input/output program development.

The work described in this report was performed between October 1972 and June 1974 under AIRTASK A03P-03P2/008C.3W16-25-001.

This report contains preliminary information and must not be the basis for official action.

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LEE E. LAKIN, JR., Head
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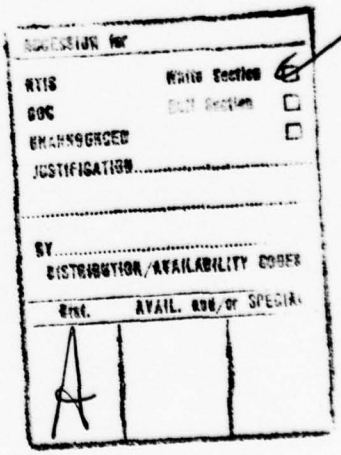

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INTRODUCTION

The Advanced Visual Target Acquisition System (AVTAS) has been developed by the Naval Weapons Center to enable the Agile weapon system to rapidly acquire an airborne target at large off-boresight angles. The pilot's task is to simply establish a good sight picture of a target and line up on that target an optical sight which is rigidly attached to the pilot's helmet. The ATVAS, which is a helmet tracker, ultimately computes the digital direction cosines in aircraft coordinates of the pilot's line of sight. These direction cosines are used to drive the Agile seeker system to rapid target acquisition.

AVTAS is an electro-optical system that uses no moving parts, is lightweight, does not restrict the pilot's movement or vision, has a wide field of view, and can be flown in high performance fighter aircraft. AVTAS has been designed for use in both laboratory and flight test programs to evaluate the operational characteristics of the system. Figure 1 illustrates the system concept, and Figure 2 shows the installation technique in a F4 aircraft.

SYSTEM DESCRIPTION

The AVTAS consists of four basic subsystems. These are the Honeywell HDC 601C avionics computer, the computer interface, the helmet with four Light Emitting Diodes (LED's) and drive circuitry, and the four dual-axis position sensing photodetectors and associated electronic circuits. Figure 3 is a simplified block diagram of AVTAS showing the basic system components.

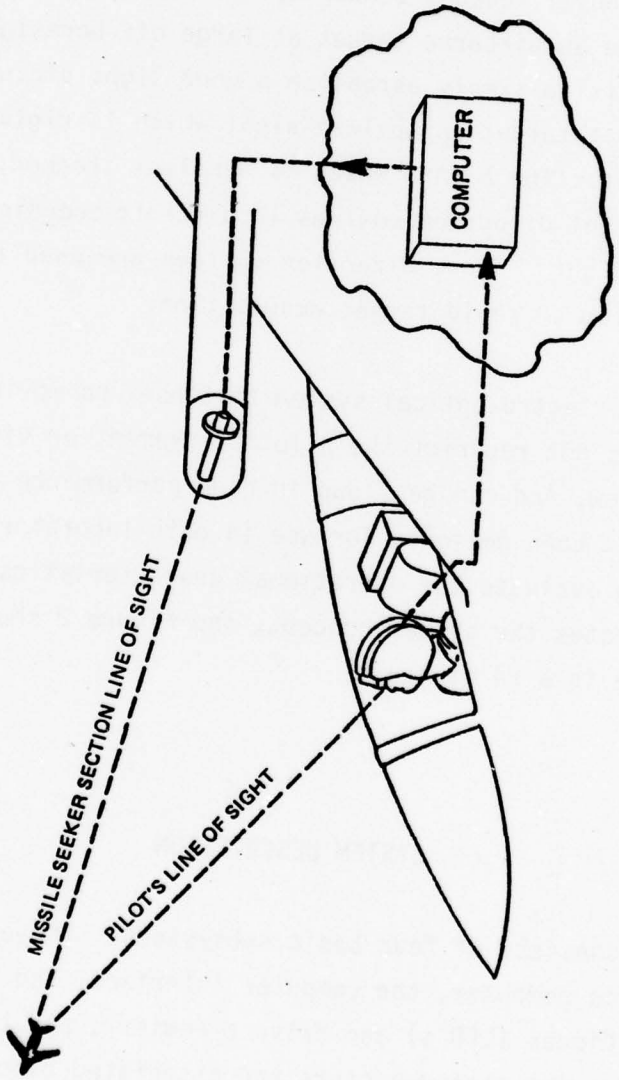

FIGURE 1. AVTAS Acquisition and Tracking.

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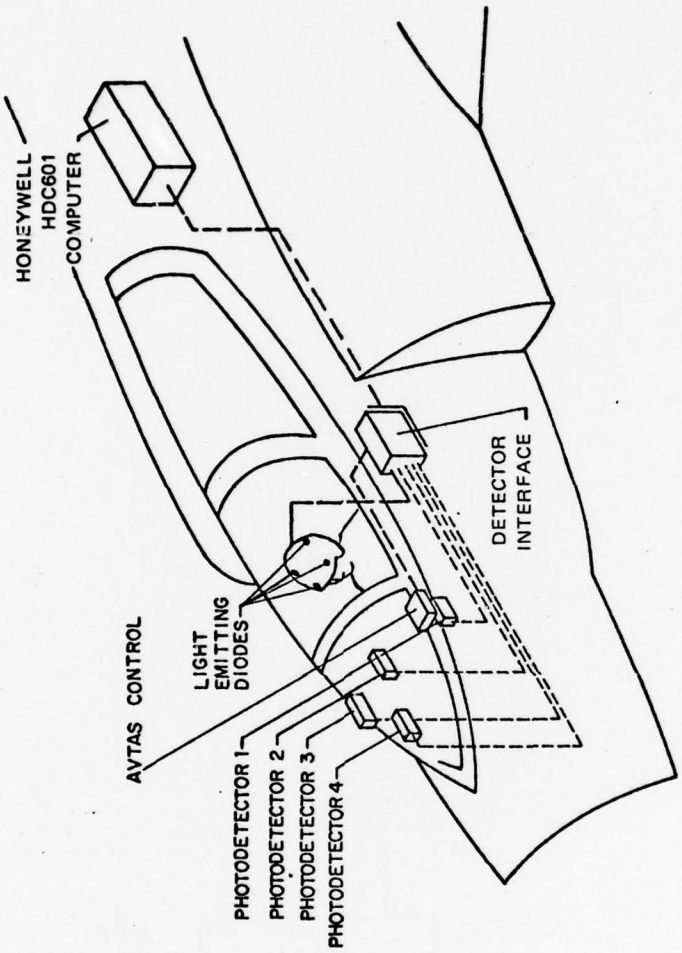

FIGURE 2. AVTAS Installation, F4 Aircraft.

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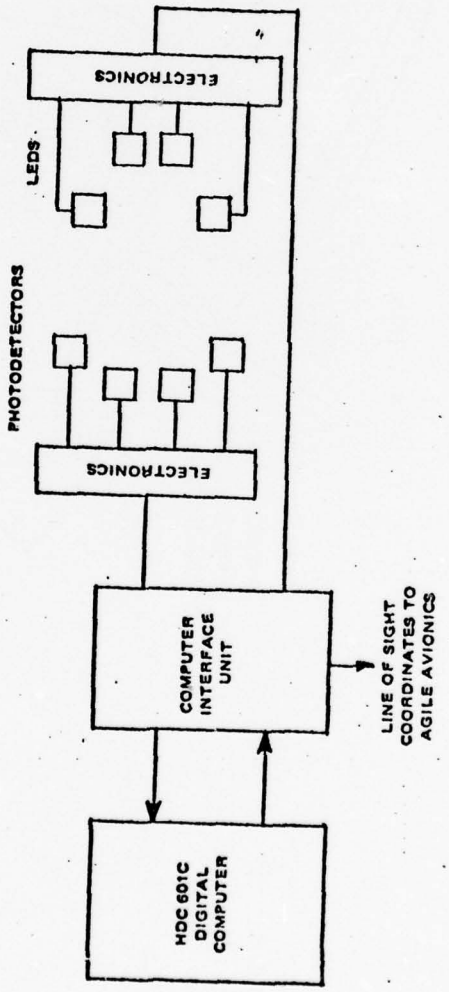

FIGURE 3. Simplified Block Diagram of AVTAS.

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The Computer Interface (CI) unit provides control and data signal lines which electrically link the computer with the remainder of the system. Serial channels are used for the transmission of data between the LED/Detector electronics and the CI and to the Agile Avionics equipment which is external to the system.

The major part of the electronics associated with the photodetector and the LED's has been combined in an enclosure called the Detector Interface (DI) unit. This includes the LED driver circuits, the synchronous filters, and the multiplexer/A-D converter. The DI has been designed to be mounted in the cockpit area (MAP BOX) to minimize the length of the cable runs to the helmet and the photodetectors.

A simplified diagram depicting the various components of the system and the signal paths which are used to transfer the data from one part to another is shown in Figure 4.

Two additional components, the Power Supply (PS) unit and the Control Panel, complete the basic system. All of the power required by the system is supplied by the three power supplies contained in the PS unit. The system operating controls are provided on the Control Panel, which will be mounted in the cockpit area.

To facilitate computer program development and system performance evaluation, a Computer Control Unit with an ASR-33 teletype, a high-speed punched tape reader, and an azimuth-elevation (Az-El) display are included in the laboratory configuration. The laboratory system is shown in block diagram format in Figure 5. The Computer Control Unit permits operational control of the HDC 601 while the punched tape reader and teletype are used for program development as well as the checkout of the system. The Az-El display provides in real-time the orientation angles of the LED array, which have been computed by the HDC 601C, located either on the helmet or on one of the test fixtures.

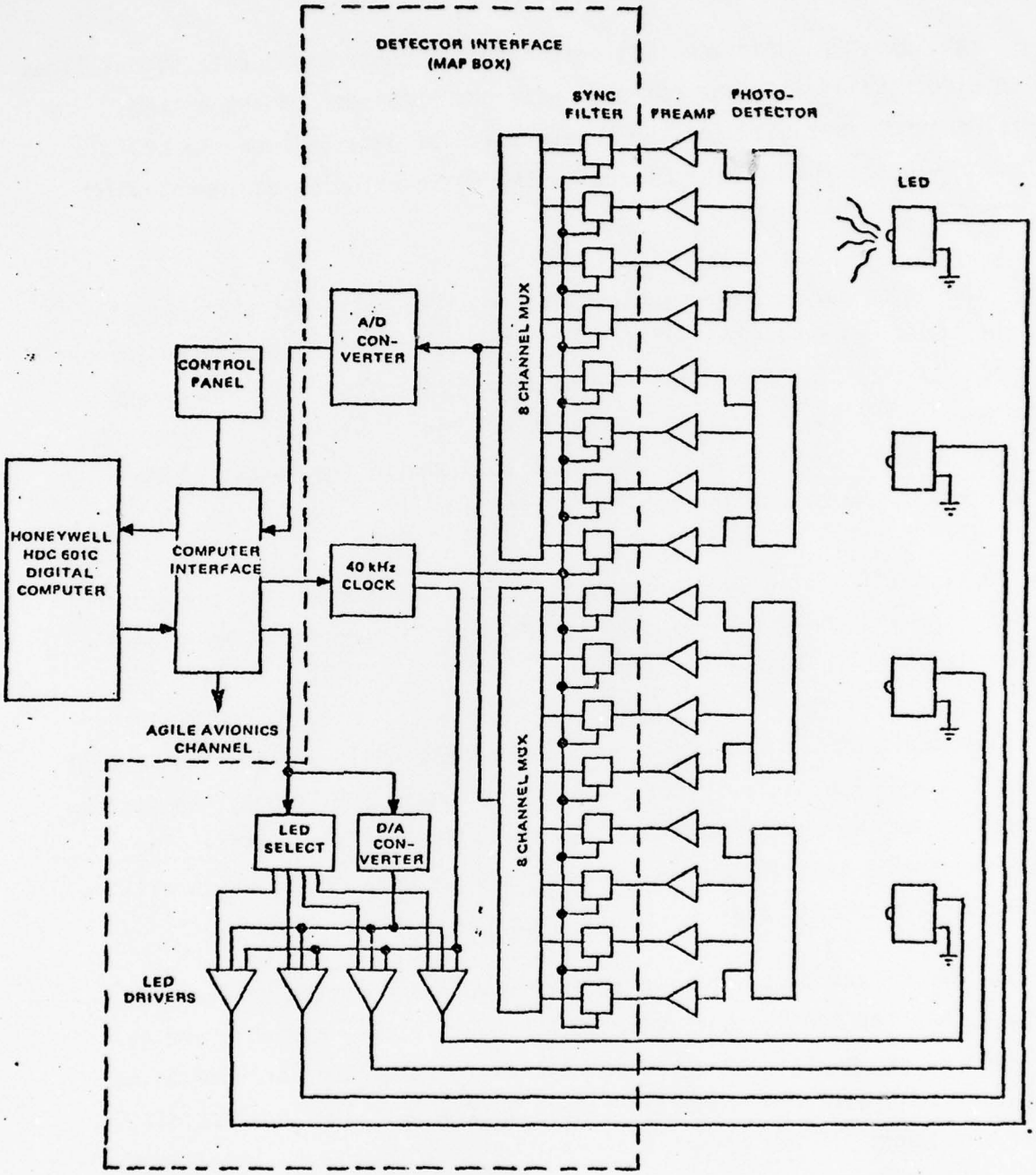

FIGURE 4. Simplified Diagram of Signal Flow for AVTAS.

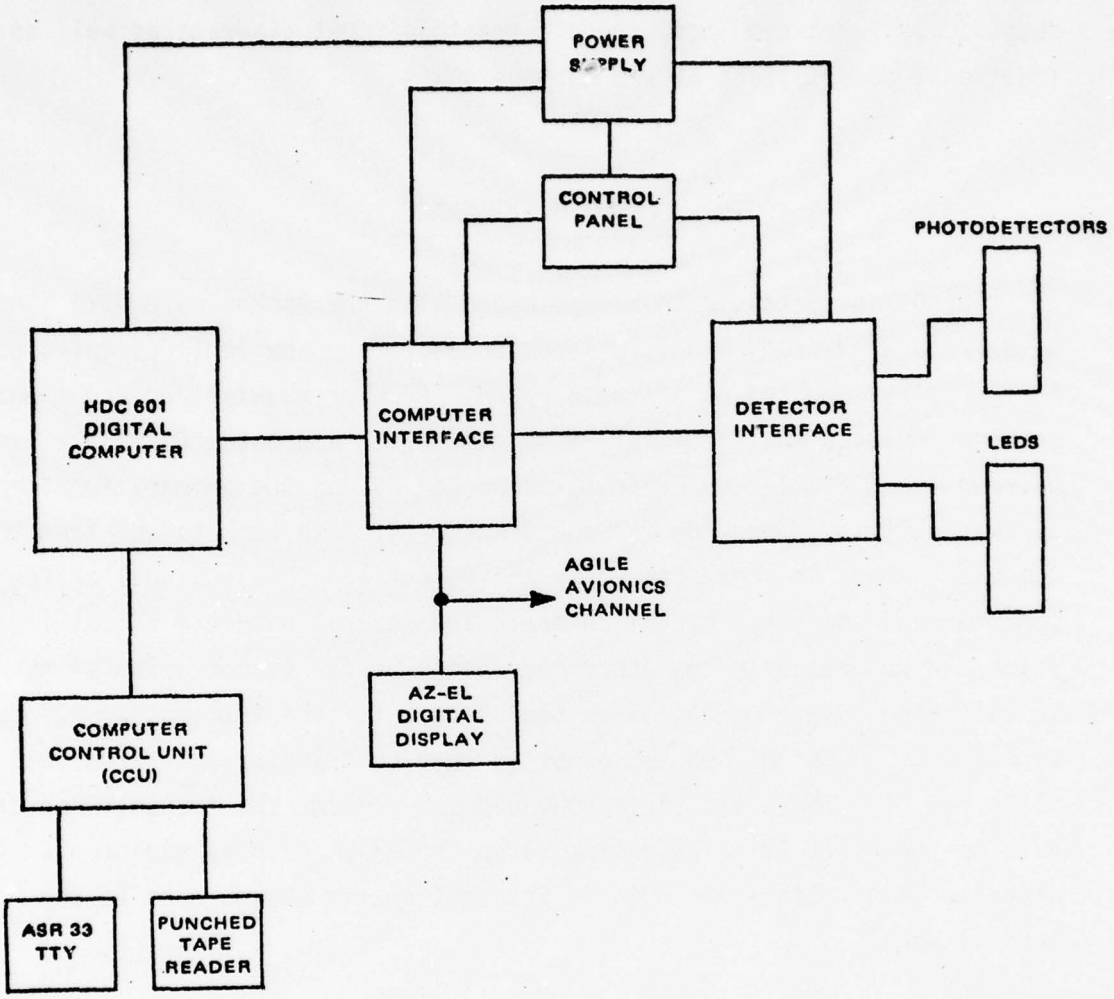

FIGURE 5. Laboratory Configuration of AVTAS.

The following sections discuss the components of AVTAS in greater detail. Included are logic and electronic circuit diagrams as well as functional descriptions of the various units.

COMPUTER INTERFACE

The CI is contained in an enclosure with the approximate dimensions of 8-1/2"W X 13-3/8"H X 3"D, without connectors. The logic circuits used in the CI are mounted on a single board. A power regulator circuit board is also included for the local +5 volt supply. Since the CI is the link between the HDC 601 and other parts of the AVTAS, the primary function of this unit is to provide for the transfer of data both to and from the computer. This is accomplished by the Direct I/O (DIO) channel on the computer end and three serial channels and several discrete signal lines which are connected to the other components of the system. Two of the serial channels are connected to the DI, one for the transmission of data from the CI to the DI and the other is used to transfer data from the DI to the CI. The third serial channel is used for the transmission of data to the Agile Avionics equipment or the AZ-EL display equipment. The discrete signal lines are used to transmit system status data to the control panel.

Figure 6 shows a simplified diagram of the flow of data through the CI. The basic timing clocks used throughout the system are also generated in the CI. Four timing signals are sent from the CI to the DI. These include the basic 4 MHz clock and three 40 KHz clocks.

DIO CHANNEL

The DIO channel on the HDC 601 consists of two parallel I/O data busses of 16 bits each, a 10-bit address bus, various control lines, and

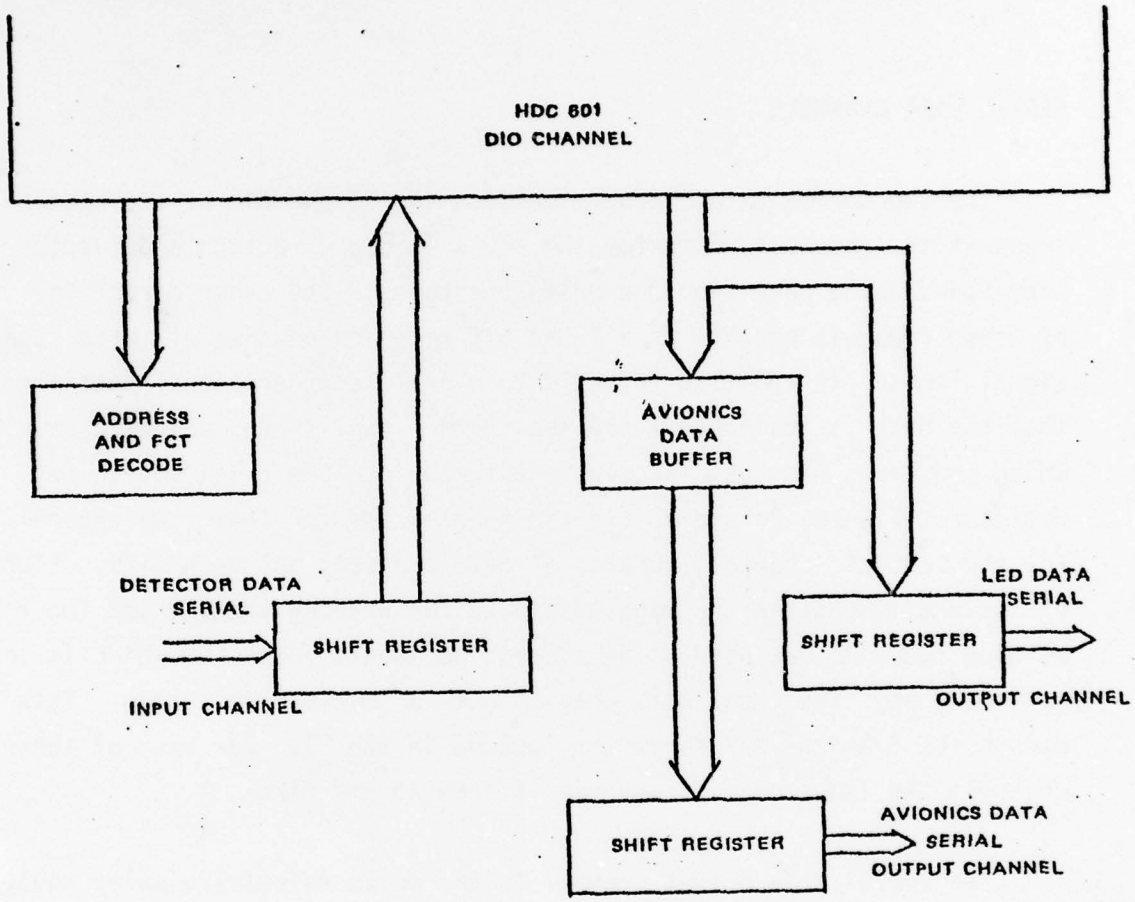

FIGURE 6. Simplified Diagram of Data Flow Through Computer Interface.

a computer interrupt. A detailed description of this channel can be found in the HDC 601 Input/Output Manual.[1/]

SERIAL DATA CHANNELS

The two serial data channels between the CI and the DI are used to transmit the intensity data for the LED's in one direction and receive the converted analog data from the photodetectors in the other direction. Both of these channels operate at a 1-MHz bit rate and consist of three separate signal lines. In addition to the data signal, another signal specifies that the data is available while the third signal serves as the data clock which indicates when data should be entered into the receiving shift register. Figures 7a and 7b are timing diagrams for these two channels. For the LED data channel, 10 bits of data are sent out each time. Eight of these bits contain the magnitude data for driving the LED and the remaining two bits are used as an address to identify the LED which is to be turned on. The input data channel uses a 12-bit data format. This data comes from the A/D converter located in the DI. For both of these channels the least significant bit is transferred first.

The serial data output channel to the Agile Avionics/Display equipment is used for the transmission of the Line-of-Sight data which includes the azimuth and elevation angles along with the X, Y and Z direction cosines. The Avionics data consists of six words of 12 bits each. The timing diagram for this serial channel is shown in Figure 7c. This channel has a fourth signal in addition to the three mentioned above for the serial channels. This signal is called End of Transmission and indicates when all of the six words have been transmitted. The data

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1/ Honeywell Aerospace Division. "HDC-601 Input/Output Manual", Sept 1972.

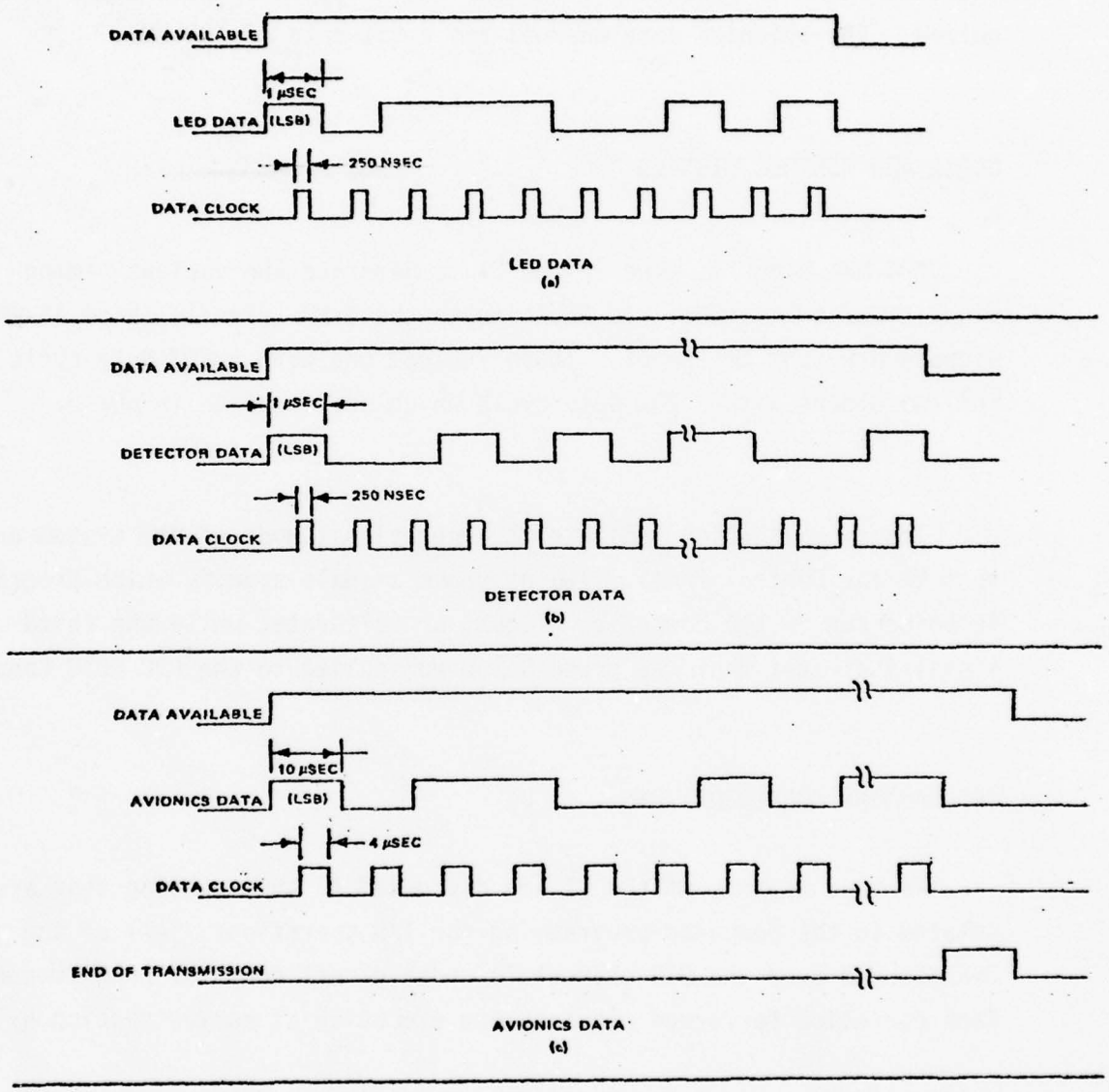


FIGURE 7. Serial Data Timing Diagrams.

for five of the six words have been designated. These include: azimuth, elevation, X-direction cosine, Y-direction cosine, and Z-direction cosine. The sixth word is presently blank and can be used for future growth if required. The avionics data channel has a bit rate of 100 KHz.

CLOCK AND CONTROL SIGNALS

A 4-MHz clock is used in the CI to generate the various timing signals for the system. In addition to the 4-MHz signal, three 40-KHz signals are sent to the DI. These include one with a 50% duty cycle and two others with a 20% duty cycle which are opposite in phase.

The signals which indicate the operational mode of the system are sent to the Control Panel. Two of these signals specify which program is being run in the computer, flight, or calibrate; while the third signal indicates that the power has been applied to the HDC 601C Computer.

PROGRAMMING CONSIDERATIONS

Various aspects of the CI are discussed in this section that are related to the computer programming for I/O operations. All of the data transferred over the DIO channel is under direct computer program control. Each operation performed requires the execution of an instruction by the

computer. Detailed information on the I/O instructions can be found in the HDC 601 Programmer's Reference Manual.[2/] The CI has been designed to use output commands from the HDC 601C to set up specific I/O operating modes or to perform designated functions. These commands have been separated into two groups. The commands associated with the first group, listed in Table 1, control the clock operations and the system operating mode indicators. The device address for this group is '06'. The second group of commands controls the I/O transfer of data and the system reset. This group is listed in Table 2 and has the device address of '07'.

The clock control commands are used to provide a real time clock and to control the sample and hold operations of the synchronous filters which are located in the DI. A counter has been implemented in the CI to indicate an elapsed time of one millisecond. The output commands initiate the operation of this counter as many times as required to obtain the desired interval in one millisecond increments. The completion of the period is indicated by both a status signal and an interrupt signal to the computer if the interrupt mask has been set. The counter interrupt mask bit is OTB13.

The start/stop commands for the 40 kHz sample signals determine when the synchronous filter circuits are sampling the output signals from the photodetectors or holding the signals obtained until they can be multiplexed and converted by the A/D converter.

[2/] Honeywell Aerospace Division. "HDC-601 Digital Computer Programmer Reference Manual." Sept 1972, Publication No. 28259.

TABLE 1. Clock and Indicator Control Commands.

Commands	Function Code
Start 40K Hz Sample Signal (STSS)	0001
Stop 40K Hz Sample Signal (SPSS)	0010
Start 1 msec Counter (STMC)	0011
Stop 1 msec Counter SPMC)	0100
Activate Flight Light (AFLT)	0101
Activate Calibrate Light (ACLT)	0110
Turn On Reticle Light (ONRL)	0111
Turn Off Reticle Light (OFRL)	1000
Skip If Counter Not Busy	1100
Skip If Counter Done	1101
Skip If Counter Not Interrupting	1110

TABLE 2. Input/Output Mode Control Commands.

Command	Function Code
Reset System (RSYM)	0001
Set LED Data Output Mode (SLDM)	0010
Reset LED Data Output Mode (RLDM)	0011
Set Agile Avionics Data Output Mode (SADM)	0100
Reset Agile Avionics Data Output Mode (RADM)	0101
Set Detector Data Input Mode (SDDM)	0110
Reset Detector Data Input Mode (RDDM)	0111
Start A/D Converter (SADC)	1000
Skip If LED Data Ready	1011
Skip If Agile Avionics Data Ready	1100
Skip If Detector Data Ready	1101
Skip If Detector Data Not Interrupting	1110

Detector Data Interrupt Mask Bit: OTB03

The three signals which indicate the status of the operation of the system are all controlled by output commands. To turn on either the Flight or Calibrate light and keep it on requires the program to generate an output command at a minimum rate of two times a second. The light will turn off approximately one second after receiving the last command. Provisions have been made so that the reticle light on the helmet can be controlled by the computer program. One output command is used to turn the light on and another command is used to turn it off.

The selection of the I/O mode for the transfer of the three different types of data by means of the DIO is performed by an output command. This command enables the logic in the CI to accept the LED or Agile avionics data from the computer or to load the input data bus to the computer with the converter detector data. Once a particular mode has been selected, the transfers are accomplished by a per-word basis. A separate I/O instruction must be executed by the computer to send or receive each data word.

To initiate the A/D conversion cycle for the detector data signals, a Start A/D Converter command is sent from the computer to the DI via the CI. All 16 of the detector signals are then converted, one at a time, and transmitted to the CI. Upon receipt of each word the A/D Data Ready status signal is brought high to indicate that the data is ready for transfer into the computer. If the Detector Data Interrupt Mask Bit has been set, the computer will also be interrupted upon receipt of the detector data word. The Detector Data Interrupt Mask bit is OTB03.

The status signals used to indicate when the CI is able to accept data from the computer are LED Data Ready and Agile Avionics Data Ready. The status is automatically tested by the computer during the execution of each INA or OTA instruction. If the status signal is high, the transfer will take place and the next instruction in the program will be skipped. If the status signal is low, the program will step to the next instruction.

The formats for the I/O data are included in Figure 8. The contents of the third word of the Agile Avionics data have not been determined at this time and can be used for future growth if required.

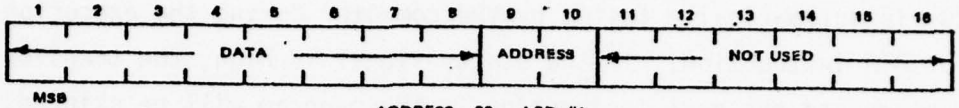
The data transfer rate for the three serial data channels is different for each of the channels. After the LED or Agile Avionics Data is sent out to the CI from the computer, additional outputs are locked out until all of the data are transmitted to the external device. Since only one LED data word is transmitted, the time required before additional data can be received from the computer is short, approximately 12 μsec. The Agile Avionics Data takes longer, however, because six words are transmitted and the bit rate is slower. The time required to transmit the Agile Avionics Data is approximately 730 μsec. The time between data word transfers for the A/D converted detector data is a minimum of 37 μsec. This includes the 25 μsec required by the A/D converter and a minimum of 12 μsec to transmit the word from the DI to the CI.

COMPUTER INTERFACE SIGNAL PIN ASSIGNMENTS

The signal pin assignments for the connectors associated with the CI are shown in Table 3. The connections between the CI and the HDC 601C utilize a single line transmission system for each signal. A two-wire, twisted pair system is used for each signal to interconnect the CI to the other equipment used in AVTAS.

LED DATA

OUTPUT BUS



ADDRESS 00 LED #1
01 LED #2
10 LED #3
11 LED #4

(a)

AGILE AVIONICS DATA

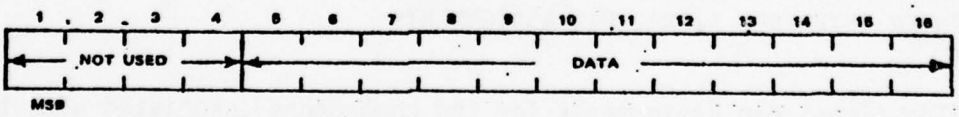
OUTPUT BUS

ADDRESS 001 AZIMUTH
010 ELEVATION
011 - -
100 X-DIRECTION COSINE
101 Y-DIRECTION COSINE
110 Z-DIRECTION COSINE

(b)

PHOTODETECTOR DATA

INPUT BUS



(c)

FIGURE 8. I/O Data Formats.

TABLE 3. Computer Interface Signal Pin Assignment.

Pin number	DIO signal name	Power signal name	Control panel signal name	Detector interface signal name	Agile avionics signal name
1	...	+10 V	Calib. indicator	Detector data	Avionics data
2	...	...	Calib. indicator	Detector data	Avionics data
3	...	...	Flight indicator	Start A/D conv.	Avionics data available
4	...	Power return	Flight indicator	Start A/D conv.	Avionics data available
5	INB050	...	Power on	Send detector data	End of transmission
6	INB060	...	Power on	Send detector data	End of transmission
7	INB070	...	Spare	Detector data clock	Avionics data clock
8	INB080	...	Spare	Detector data clock	Avionics data clock
9	INB090	...	...	Detector data available	System reset
10	INB100	...	...	Detector data available	System reset
11	INB110	...	...	LED data	...
12	INB120	Shield	Shield	LED data	...
13	INB130	...	...	LED data clock	...
14	INB140	...	...	LED data clock	...
15	INB150	...	...	LED data available	...
16	INB160	...	...	LED data available	...
17	OTB011	...	...	...	...
18	OTB021	...	...	...	...
19	OTB031	...	...	...	...
20	OTB041	...	...	...	...
21	OTB051	...	...	4 MHz	...
22	OTB061	...	...	4 MHz	...
23	OTB071	...	...	40 kHz	...
24	OTB081	...	...	40 kHz	...
25	OTB091	...	...	40 kHz ϕA	...
26	OTB101	...	...	40 kHz ϕA	...
27	OTB111	...	...	40 kHz ϕB	...
28	OTB121	...	...	40 kHz ϕB	...
29	OTB131	...	...	Reset system	...
30	OTB141	...	...	Reset system	...
31	OTB151	...	...	...	...
49	PIL00	...	...	...	...
50	...	...	...	...	...
51	ADB070	...	...	...	...
52	ADB080	...	...	...	...
53	ADB090	...	...	...	...
54	ADB100	...	...	...	...
55	ADB110	...	...	...	...
56	ADB120	...	...	...	...
57	ADB130	...	...	...	...
58	ADB140	...	...	...	...
59	ADB150	...	...	...	...
60	ADB160	...	...	...	...
61	OCPLS0	...	...	Shield	Shield
62	RRLIN0	...	...	...	...
63	DRLIN0	...	...	...	...
64	MSTCL0	...	...	...	...
65	...	...	...	...	...
66	...	...	...	...	...

TABLE 3. (Contd.)

Pin number	DIO signal name	Power signal name	Control panel signal name	Detector interface signal name	Agile avionics signal name
67	SMKO10	...	...	...	...
68	...	...	...	...	...
69	CPH10	...	...	...	...
70	...	...	...	...	...
71	SHIELD	...	...	...	...
72	SHIELD	...	...	...	...
73	SHIELD	...	...	...	...
74	SHIELD	...	...	...	...
75	SHIELD	...	...	...	...
76	SIGNAL GRD.	...	...	...	...
77	SIGNAL GRD.	...	...	...	...
78	SIGNAL GRD.	...	...	...	...
79	SIGNAL GRD.	...	...	...	...
80	SIGNAL GRD.	...	...	...	...
81	SIGNAL GRD.	...	...	...	...
82	SIGNAL GRD.	...	...	...	...
83	SIGNAL GRD.	...	...	...	...
84	SIGNAL GRD.	...	...	...	...
85	SIGNAL GRD.	...	...	...	...

Logic Drawings

Appendix A contains the drawings for the logic circuits used in the CI.

DETECTOR INTERFACE

The DI has been housed in an enclosure which is designed to be mounted in the forward cockpit of an F-4 aircraft. The enclosure is in a "L" shape as viewed from the top and has the dimensions of 11"W by 10"H and the depth changes from 3" on one end to 4-7/16" at the other end. These dimensions do not include the connectors.

The greatest part of the logic circuits is mounted on a single board in the DI. Interconnecting cables are provided for the transmission of signals within the DI between the logic board and the LED drivers and the synchronous filters. A single multiconductor cable is used to interconnect the DI to the CI.

All of the functions performed in the DI are controlled by the digital logic circuits. These circuits are used to receive data from and transmit data to the CI as well as initiate the sample and hold selection of analog data for conversion by the A-D converter and direct the brightness data to the appropriate LED driver circuit.

The analog data from the synchronous filters is multiplexed by two, eight-channel multiplexers, one for each pair of synchronous filter boards. Four synchronous filter circuits have been layed out on each 2-sided printed circuit boards. These four circuits are connected to the outputs from the four electrode preamplifiers associated with each of the photodetectors. Provisions have been incorporated on these boards so that the gains and offset voltages can be adjusted to compensate for variations in the outputs of each photodetector. The four circuit boards are contained within a shielded housing in the DI enclosure.

During the A/D conversion sequence, the digital logic selects the analog data from the multiplexers in numerical sequence. Channel 0 is selected first, Channel 1 next, and so on until all 16 channels have been selected and sent to the A/D converter. After the analog signal is converted, the digital data produced is transmitted over a serial data channel to the CI at a 1-megacycle bit rate. When the 12-bit data word has been transmitted, the conversion of the next analog signal is automatically started. This continues until the 16th channel has been converted, then the logic resets the channel selector counter to zero, and the operation is repeated upon the receipt of the next Start A/D Converter Command.

A buffer register is used to store the LED brightness data which is transmitted over a serial data channel from the CI. The buffer contains 10 bits of data. The two least significant bits are used for the LED address, and the remaining eight bits are used for the magnitude of the voltage which is to be sent to the LED. These eight bits are connected to the D/A converter which is located on the LED driver board. The resulting analog voltage from the converter is switched to the LED driver circuit specified by the address bits. The analog signal to the LED is modulated by a 40 kHz square wave which produces an output signal with a 50% duty cycle. Once selected, the LED remains on until new data is received from the CI or a system reset signal is detected.

Figure 9 is a schematic circuit diagram of the Quad LED Drivers with select switches and D/A converter. A 16-conductor flat ribbon cable is utilized to interconnect the LED driver board with the main control logic board.

The logic drawings for the digital circuits used in the DI are located in Appendix B.

Local voltage regulators are used in the DI to supply power for both the digital and analog circuits located in both the unit and the photodetectors. A single +5 volt regulator supplies the voltage required by the digital logic circuits, the two converters, and the LED driver circuits. Four ±15 volt regulators are used to supply power to the various analog circuits. One of the ±15 volt regulators is used with the A/D converter, the D/A converter, and the LED driver circuits. Two regulators are used with the synchronous filter circuits, and the fourth regulator is used to provide power to the photodetectors and associated preamplifiers.

Table 4 lists the signal pin assignments for all the DI connectors.

POWER SUPPLY UNIT

The Power Supply Unit contains three power supplies which provide the basic voltages that are distributed throughout the system. These three supplies produce +10 volts and ±20 volts. Also included is a latching relay that controls the power to the three power supplies. The relay is activated by a switch located on the Control Panel. Once the relay has been set to the ON position it will remain in this position until switched OFF by the Control Panel switch. Figure 10 depicts the wiring of the Power Supply Unit.

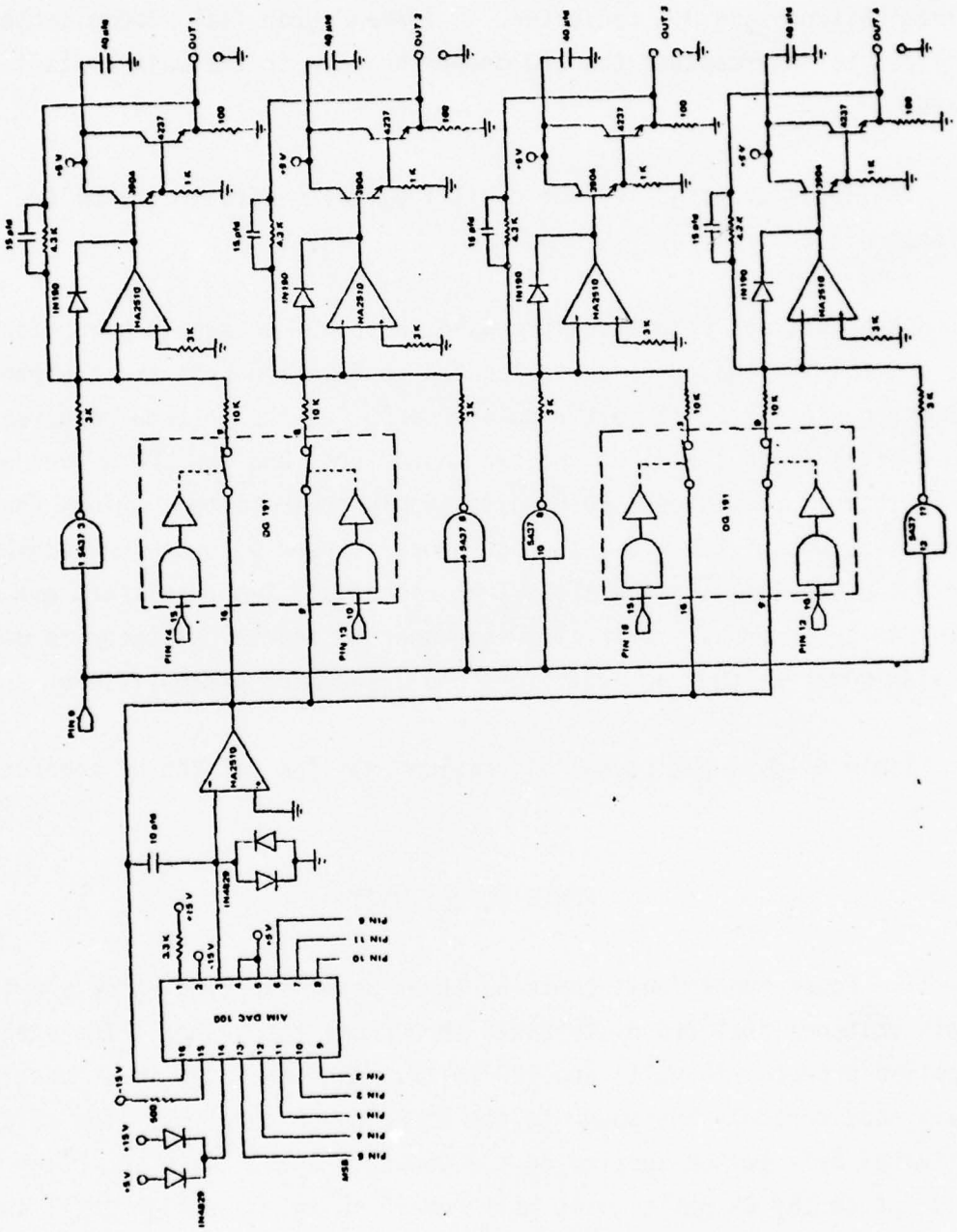


FIGURE 9. Circuit Diagram of the Quad LED Drivers.

TABLE 4. Detector Interface Signal Pin Assignments.

Pin number	Computer interface signal name	Photodetector No. 1–4 signal name	Helmet signal name	Power signal name	Control panel signal name
1	Detector data	Electrode No. 1	LED No. 1	+10 V	Unassigned
2	Detector data	Electrode No. 2	LED No. 2	−20 V	Unassigned
3	Start A/D conv.	Electrode No. 3	LED No. 3	+20 V	Unassigned
4	Start A/D conv.	Electrode No. 4	LED No. 4	Return	Unassigned
5	Send detector data	+15 V	Return	...	Unassigned
6	Send detector data	−15 V	Spare	...	Unassigned
7	Detector data clock	Return	Spare	...	Unassigned
8	Detector data clock	...	Spare	Shield	Unassigned
9	Detector data available	...	Spare	...	Unassigned
10	Detector data available	...	Spare	...	Unassigned
11	LED data	...	Spare	...	Unassigned
12	LED data	...	Spare	...	Unassigned
13	LED data clock	...	...	...	Unassigned
14	LED data clock	...	...	...	Unassigned
15	LED data available	...	...	...	Unassigned
16	LED data available	...	...	...	Unassigned
17	...	...	...	...	Unassigned
18	...	...	...	...	Unassigned
19	...	...	...	...	Unassigned
20	...	...	...	...	Unassigned
21	4 MHz	...	...	...	Unassigned
22	4 MHz	...	...	...	Unassigned
23	40 kHz	...	...	...	Unassigned
24	40 kHz	...	...	...	Unassigned
25	40 kHz ϕA	...	...	...	Unassigned
26	40 kHz ϕA	...	...	...	Unassigned
27	40 kHz ϕB	...	...	...	Unassigned
28	40 kHz ϕB	...	...	...	Unassigned
29	Reset system	...	...	...	Unassigned
30	Reset system	...	...	...	Unassigned
56	Shield	...	...	...	Unassigned

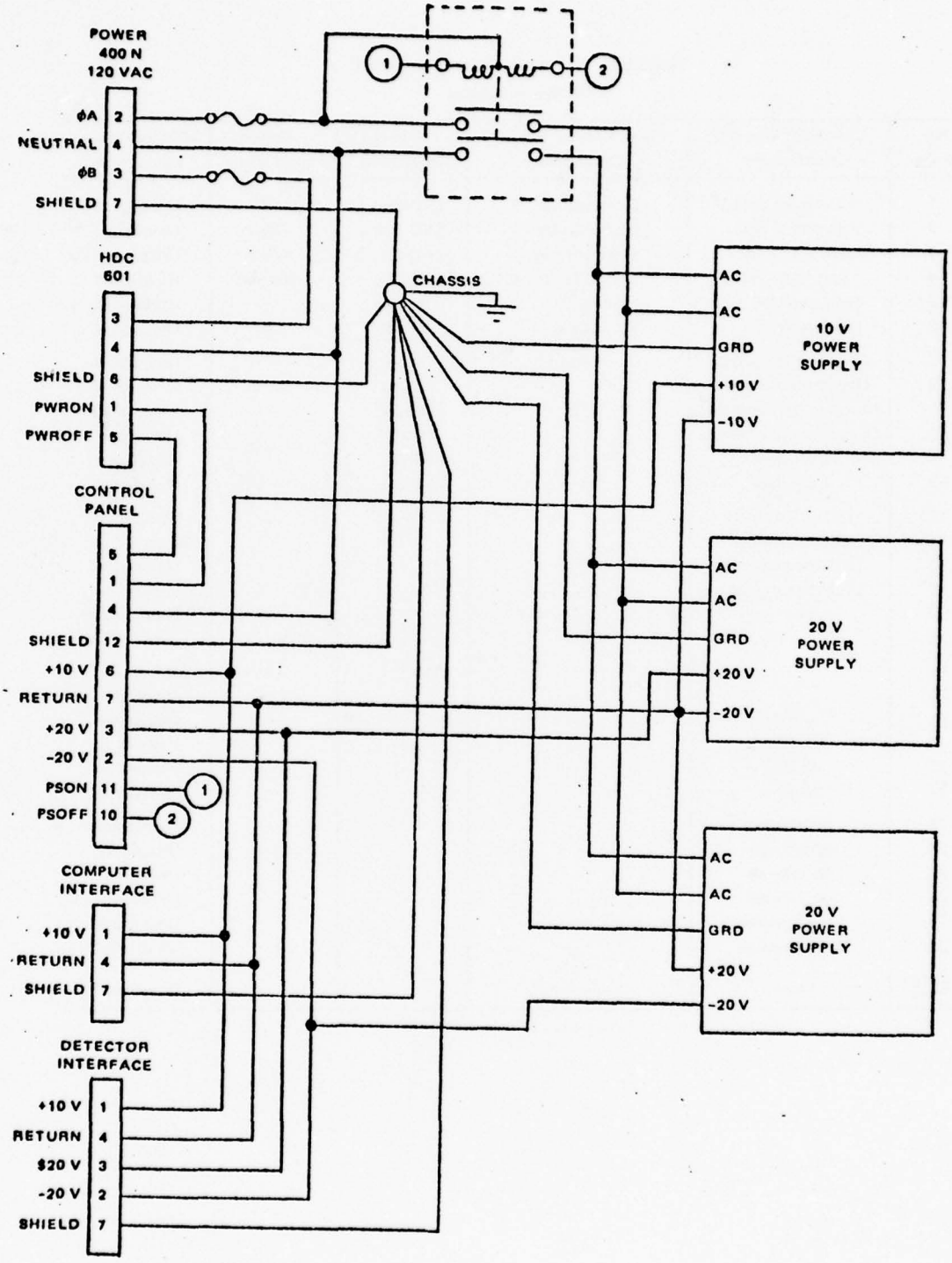


FIGURE 10. Power Supply Unit.

VOLTAGE REGULATORS

Three different circuits have been used for the voltage regulators that have been incorporated in the different parts of the system. The schematic for the +5 volt regulator used in the CI and DI is shown in Figure 11, while Figure 12 shows the circuit used in the Control Panel. The ±15 volt regulator circuit used in the DI and the Control Panel are shown in Figure 13.

CONTROL PANEL

The Control Panel contains the system and computer ON/OFF switch and four indicator lights for monitoring the status of the system. The ON/OFF switch remotely operates latching relays in both the HDC 601 computer and in the Power Supply Unit. The relays in turn control the application of power to the two devices. Two of the lights are used to show the power-on condition for the computer and the system power unit. The other two lights are used to indicate the operation of either the flight or calibrate programs in the computer.

Table 5 includes the signal pin assignments for the connectors used with the Control Panel.

Two voltage regulators are used in the Control Panel. One provides the +5 volts required by the logic and the indicators while the other provides ±15 volts which are available for the future development of the analog drive circuitry for use with the reticle and discrete lights located on the helmet.

The two control knobs are provided for intensity control of the reticle and discrete lights when the lamp drive circuitry is incorporated in the panel.

The logic circuitry used in the Control Panel is shown in Appendix C.

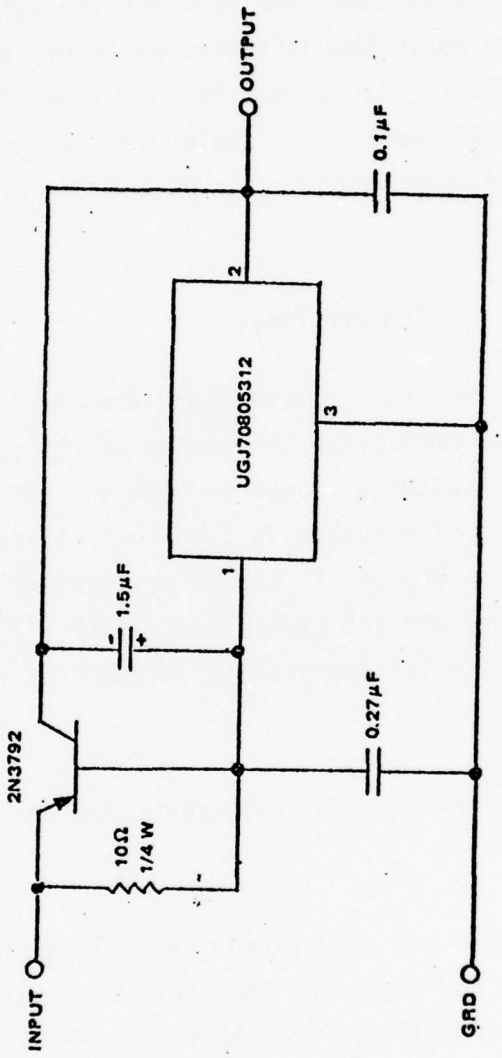


FIGURE 11. 5V Regulator Circuit 1.

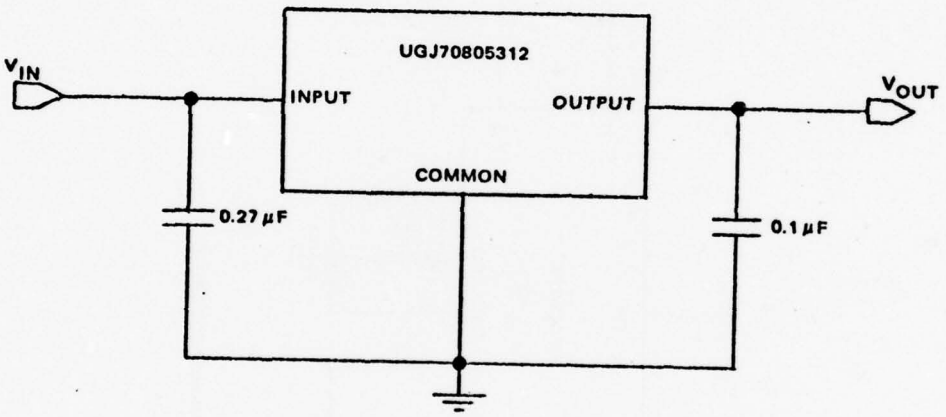


FIGURE 12. 5V Regulator Circuit 2.

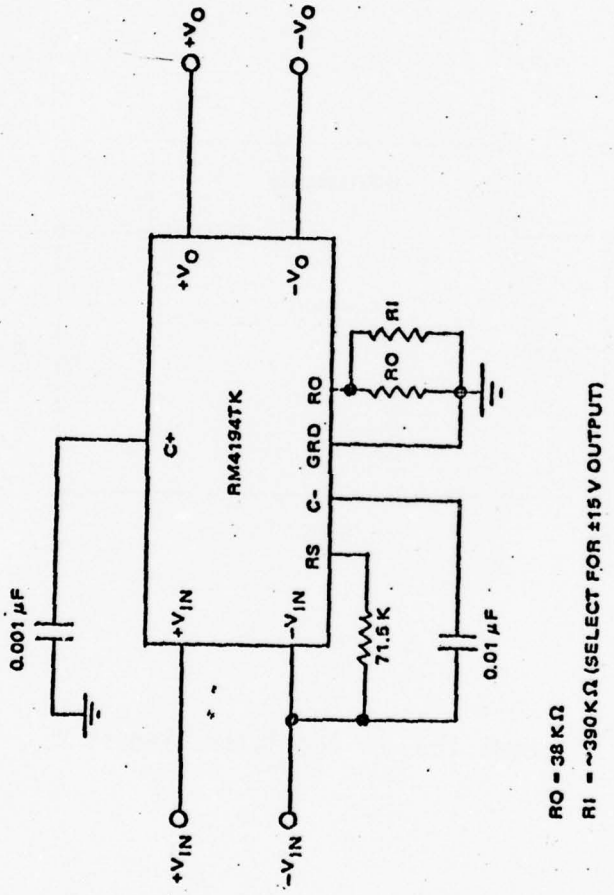


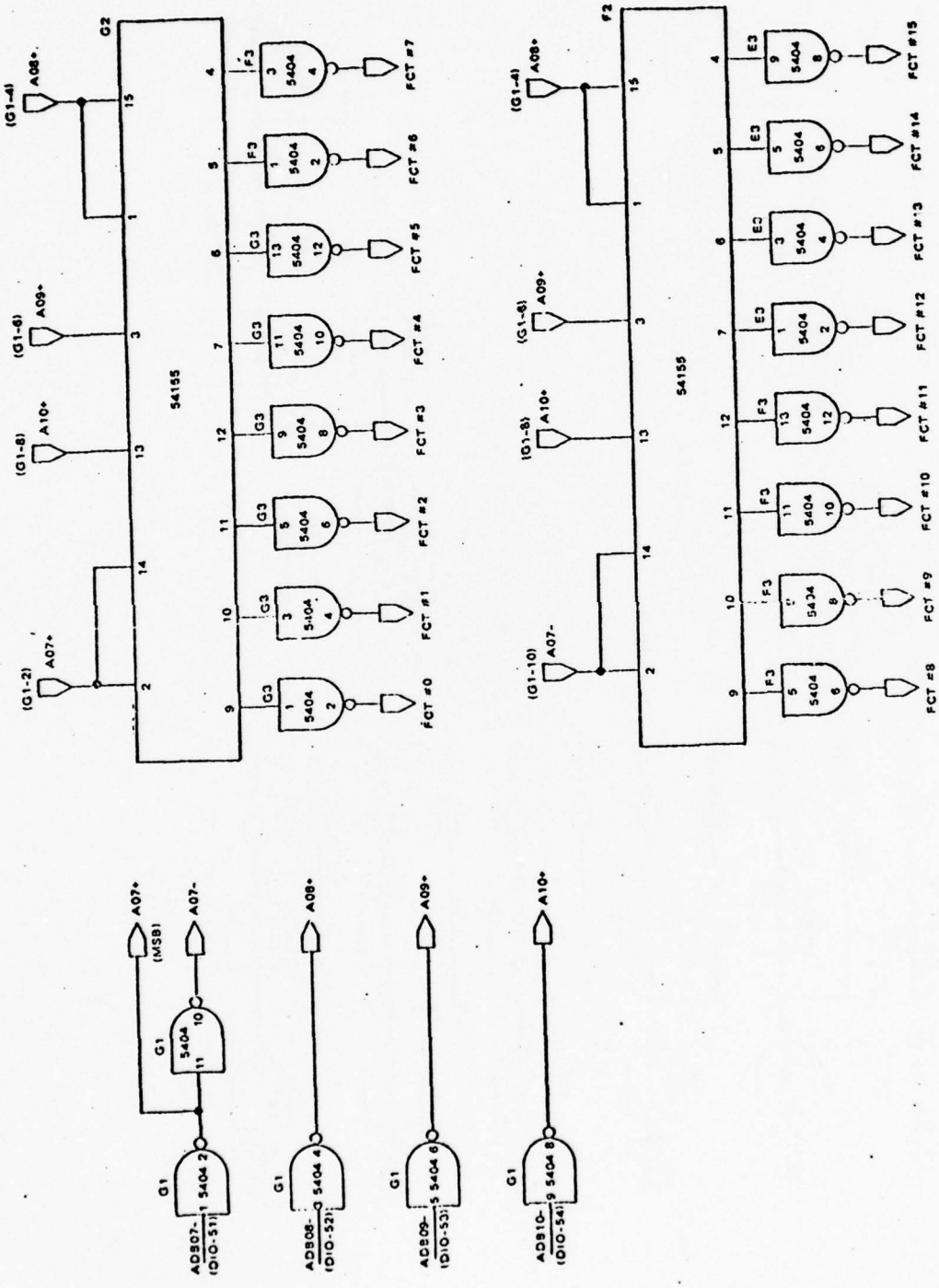
FIGURE 13. ±15 Volt Regulator Circuit.

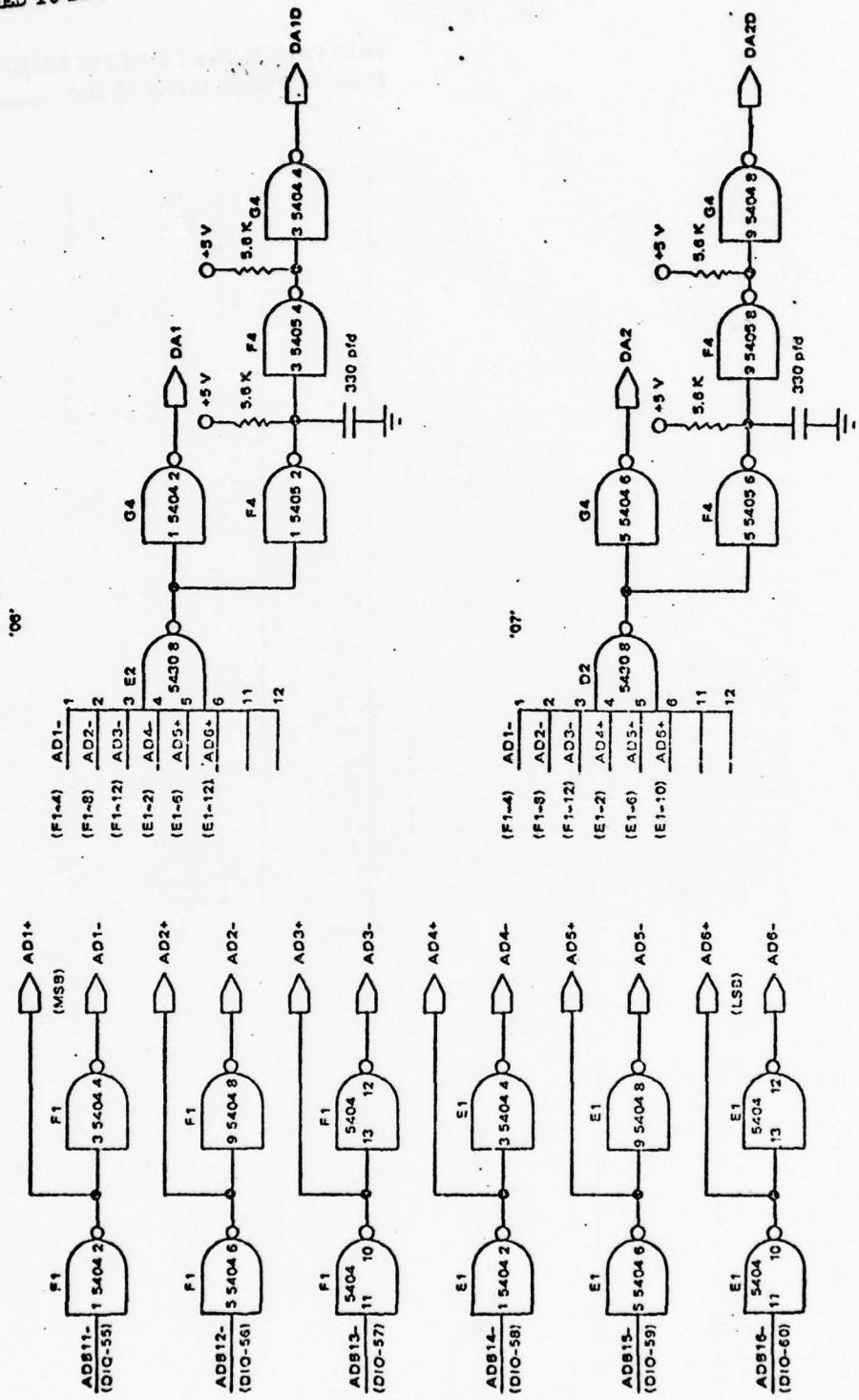
TABLE 5. Control Panel Signal Pin Assignment.

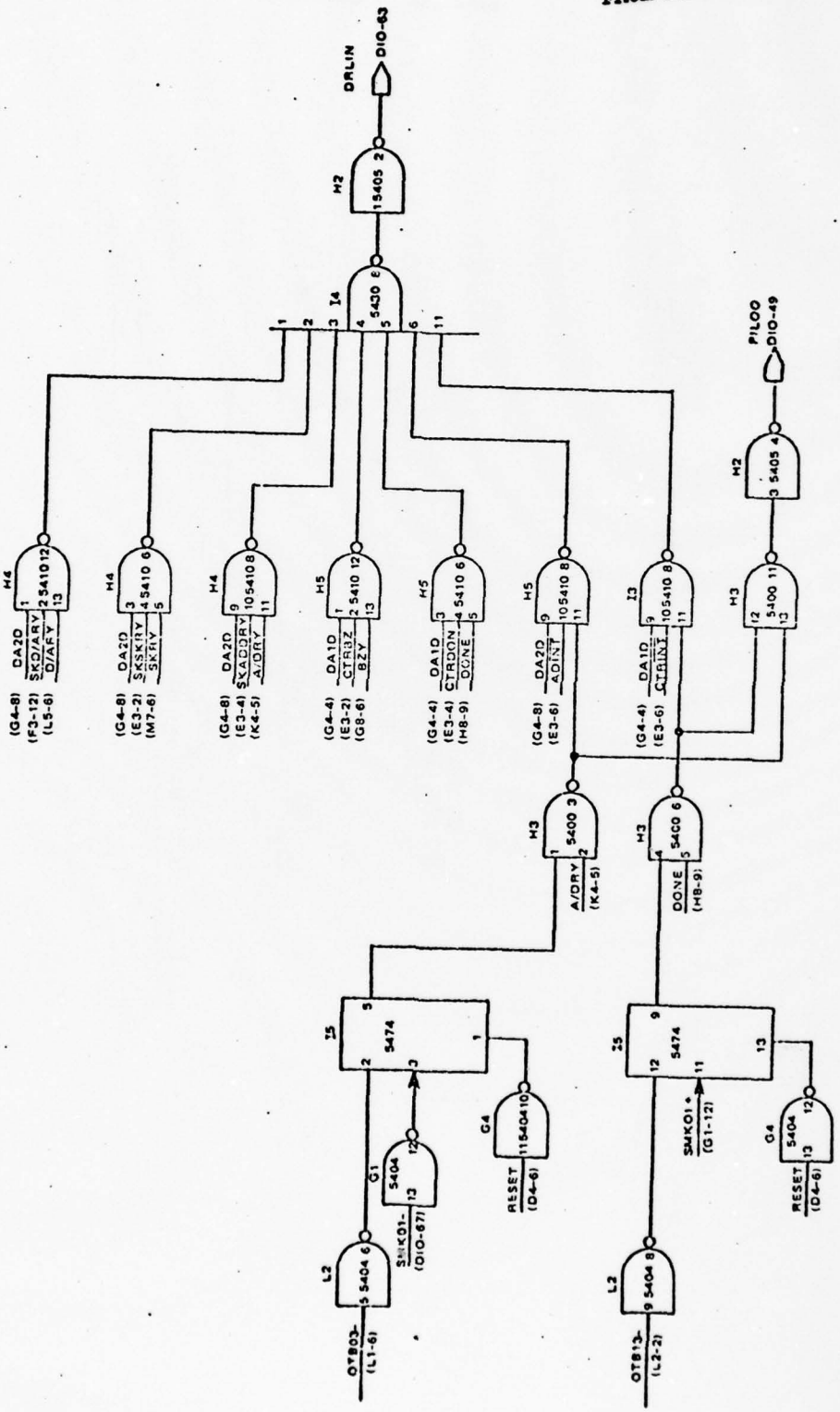
Pin number	Computer interface signal name	Ext. inputs signal name	Detector interface signal name	Power signal name
1	Calibration	Unassigned	Unassigned	Power on
2	Calibration	Unassigned	Unassigned	-20 V
3	Flight	Unassigned	Unassigned	+20 V
4	Flight	Unassigned	Unassigned	Neutral
5	Power on	Unassigned	Unassigned	Power off
6	Power on	Unassigned	Unassigned	+10 V
7	Spare	Unassigned	Unassigned	Return
8	Spare	Unassigned	Unassigned	...
9	...	Unassigned	Unassigned	...
10	...	Unassigned	Unassigned	PS off
11	...	Unassigned	Unassigned	PS on
12	Shield	Unassigned	Unassigned	Shield

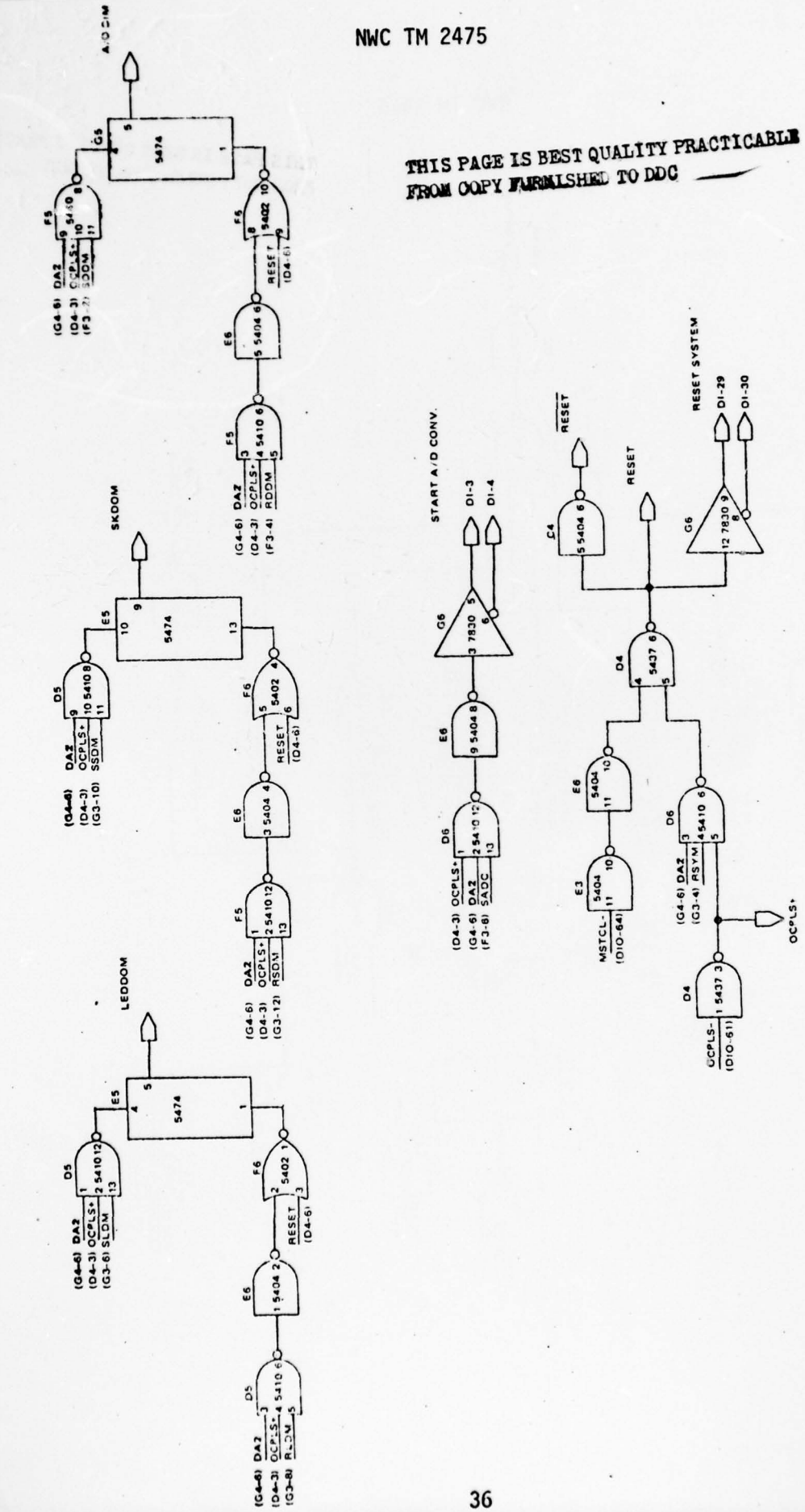
Appendix A

LOGIC DRAWINGS FOR THE COMPUTER INTERFACE









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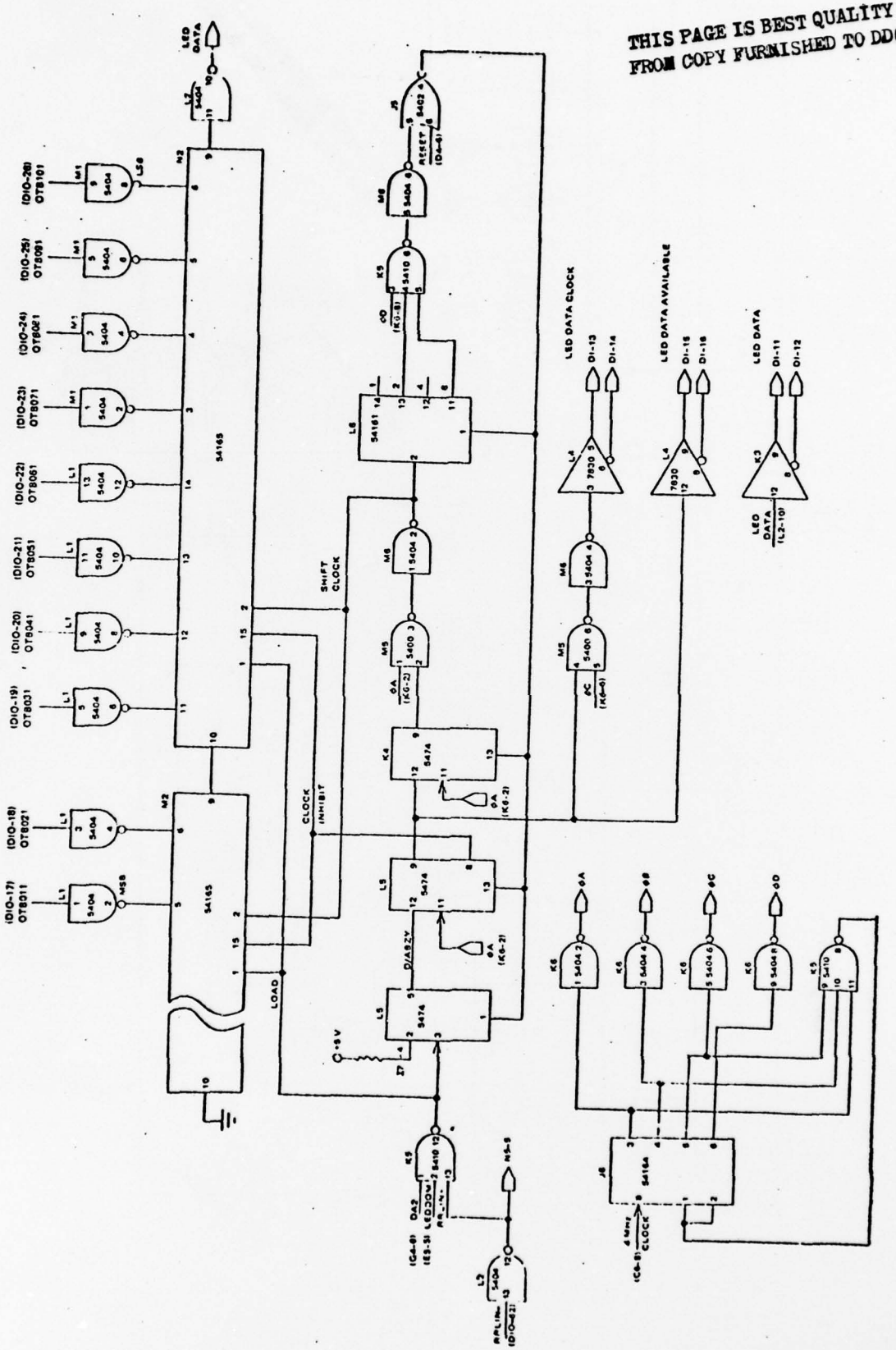

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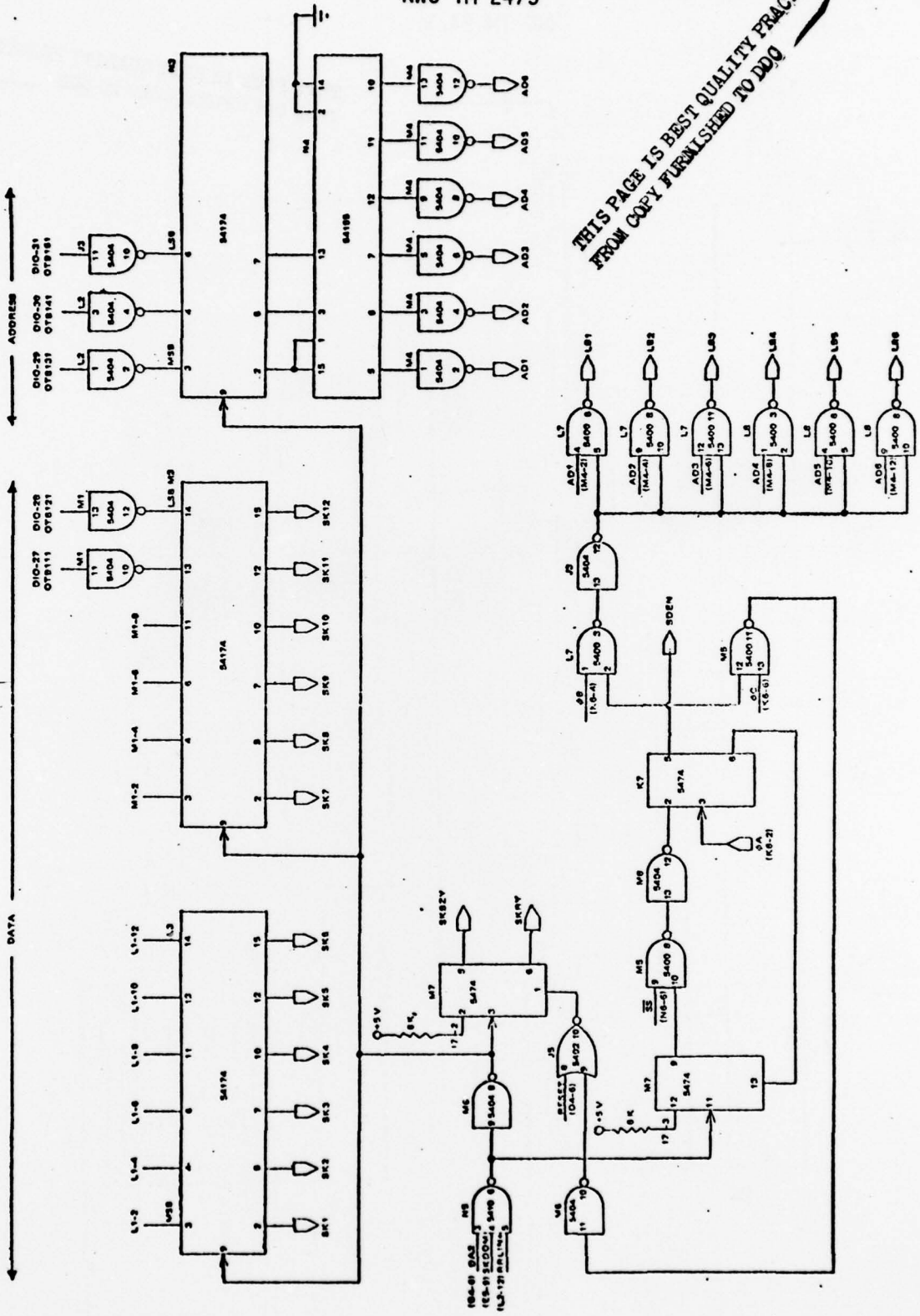

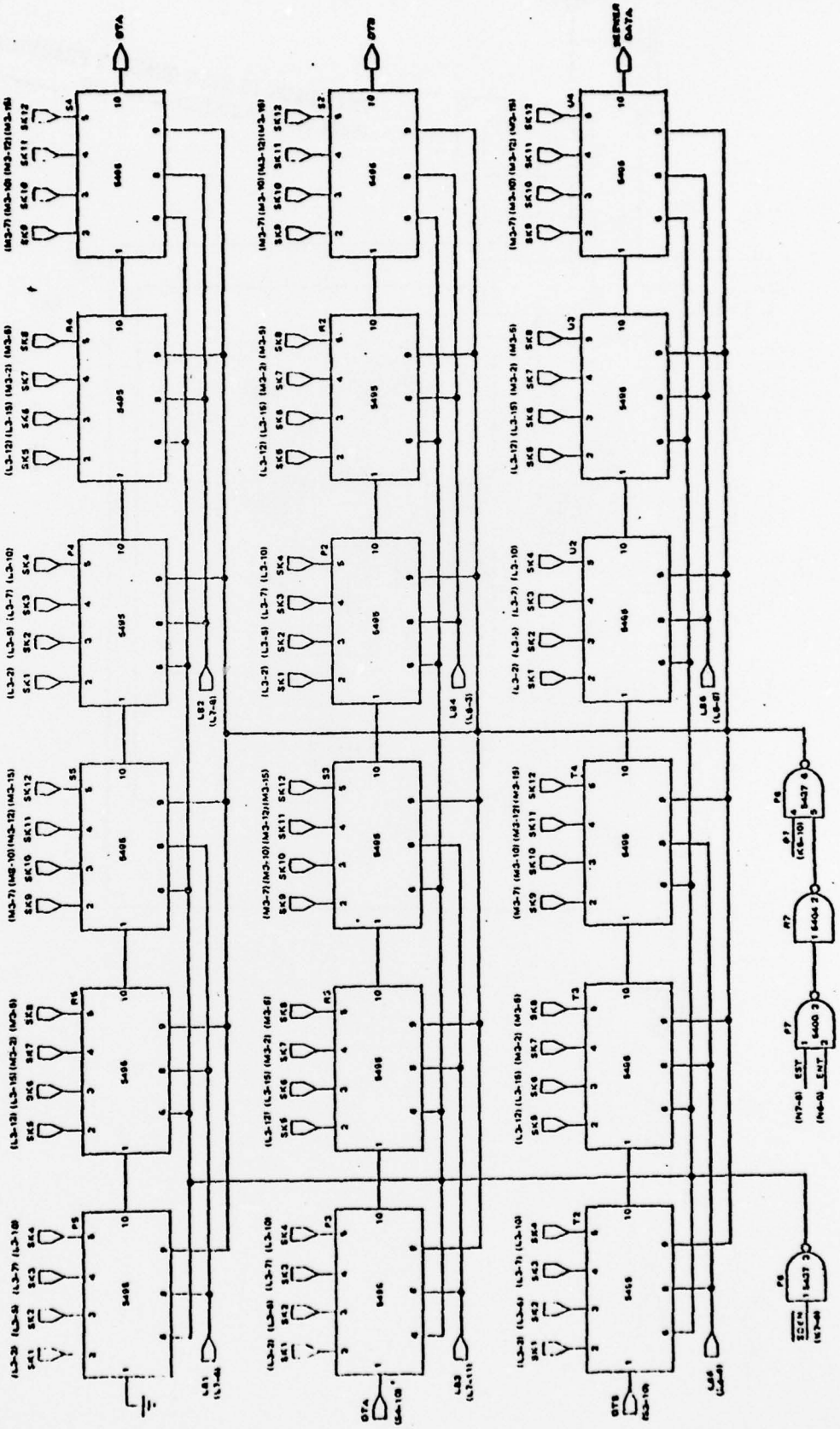

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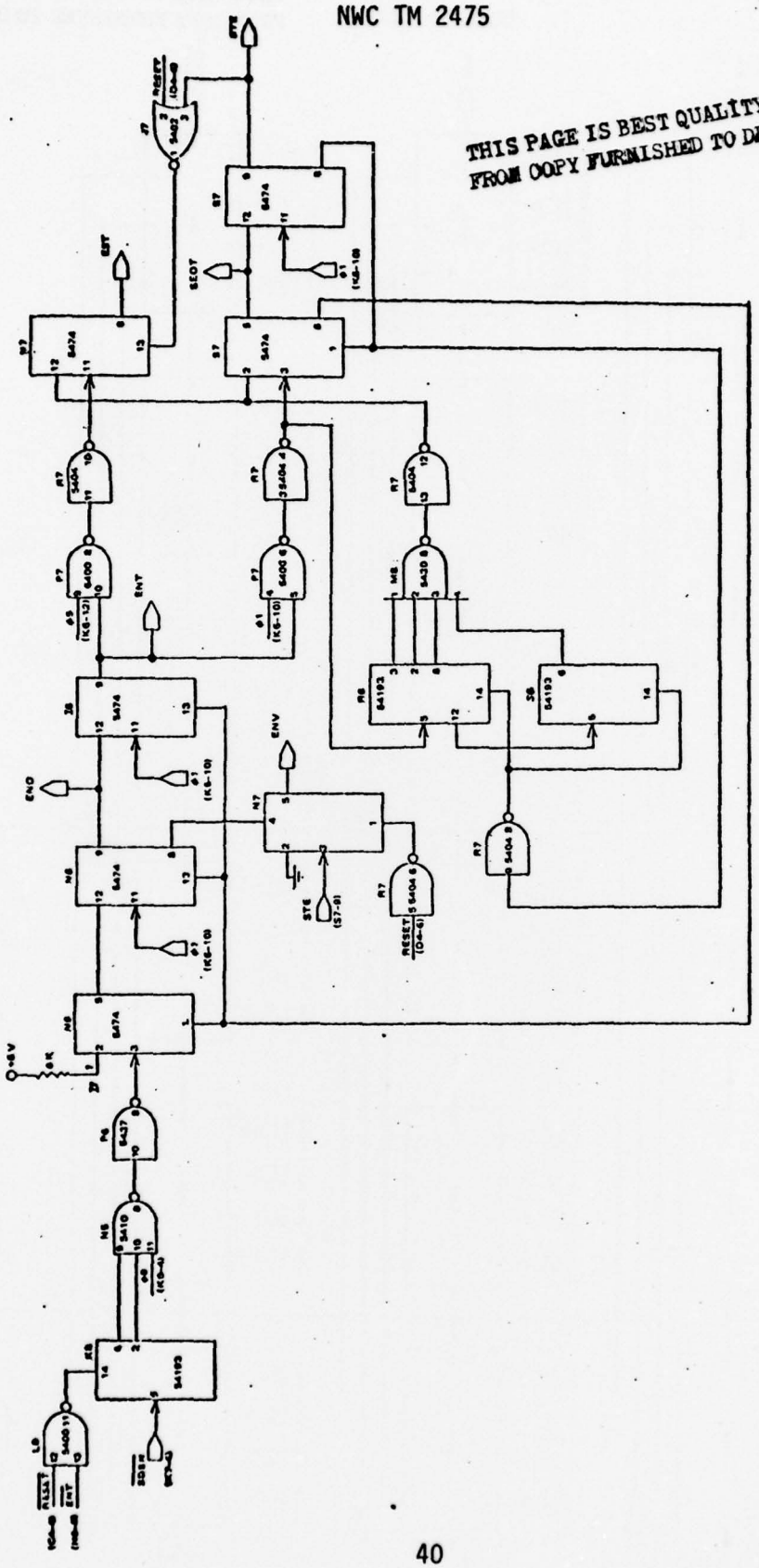

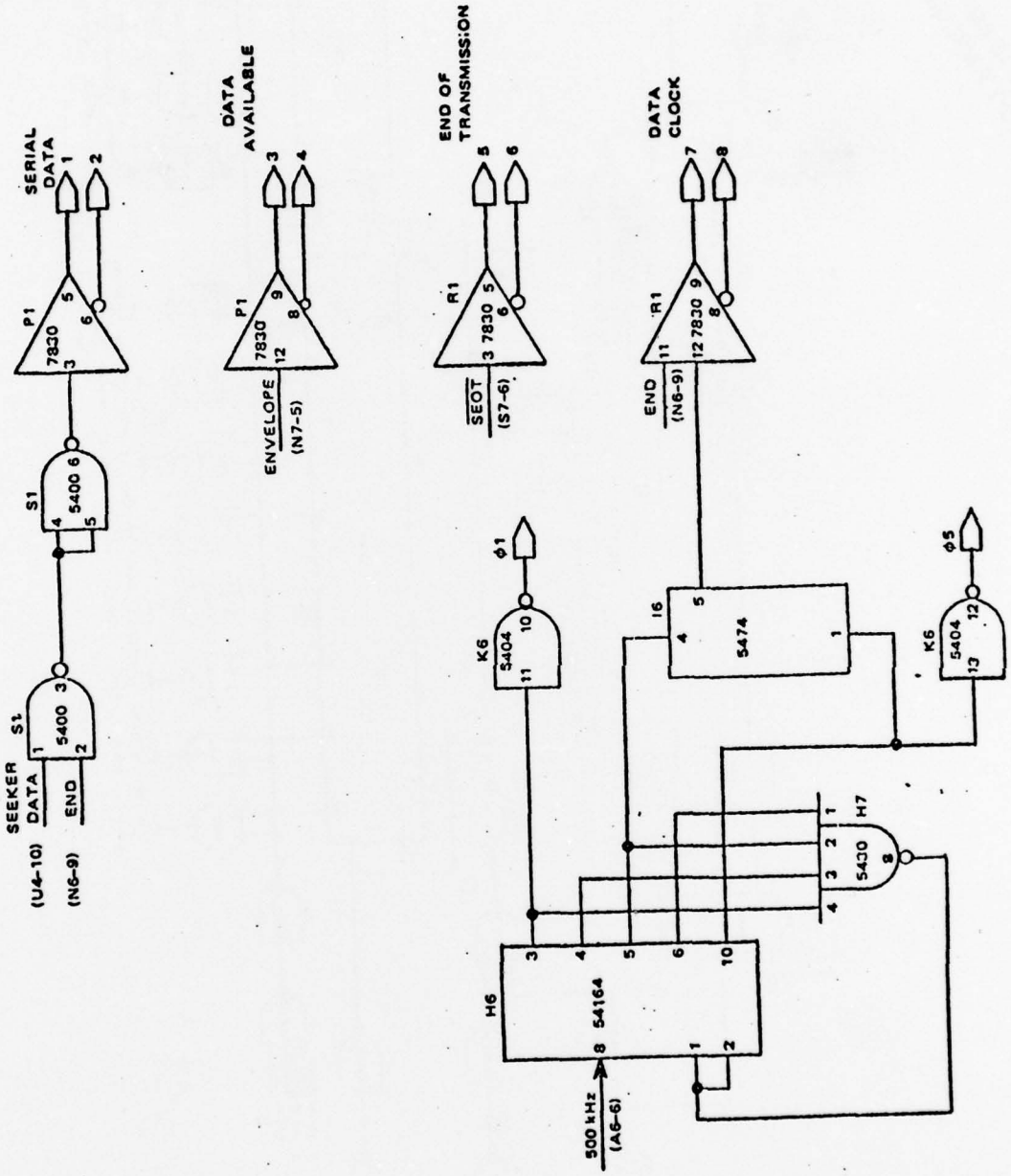

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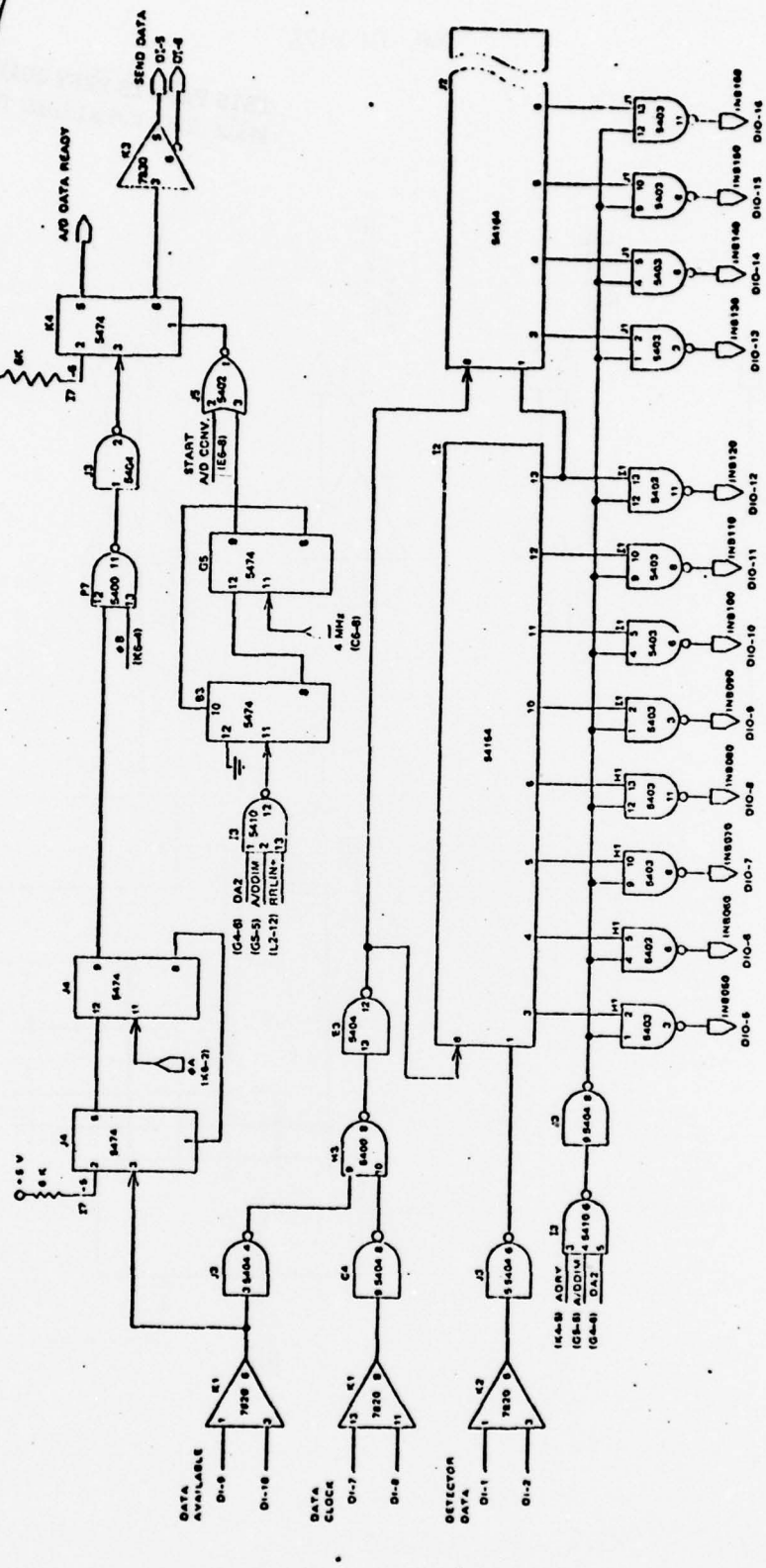

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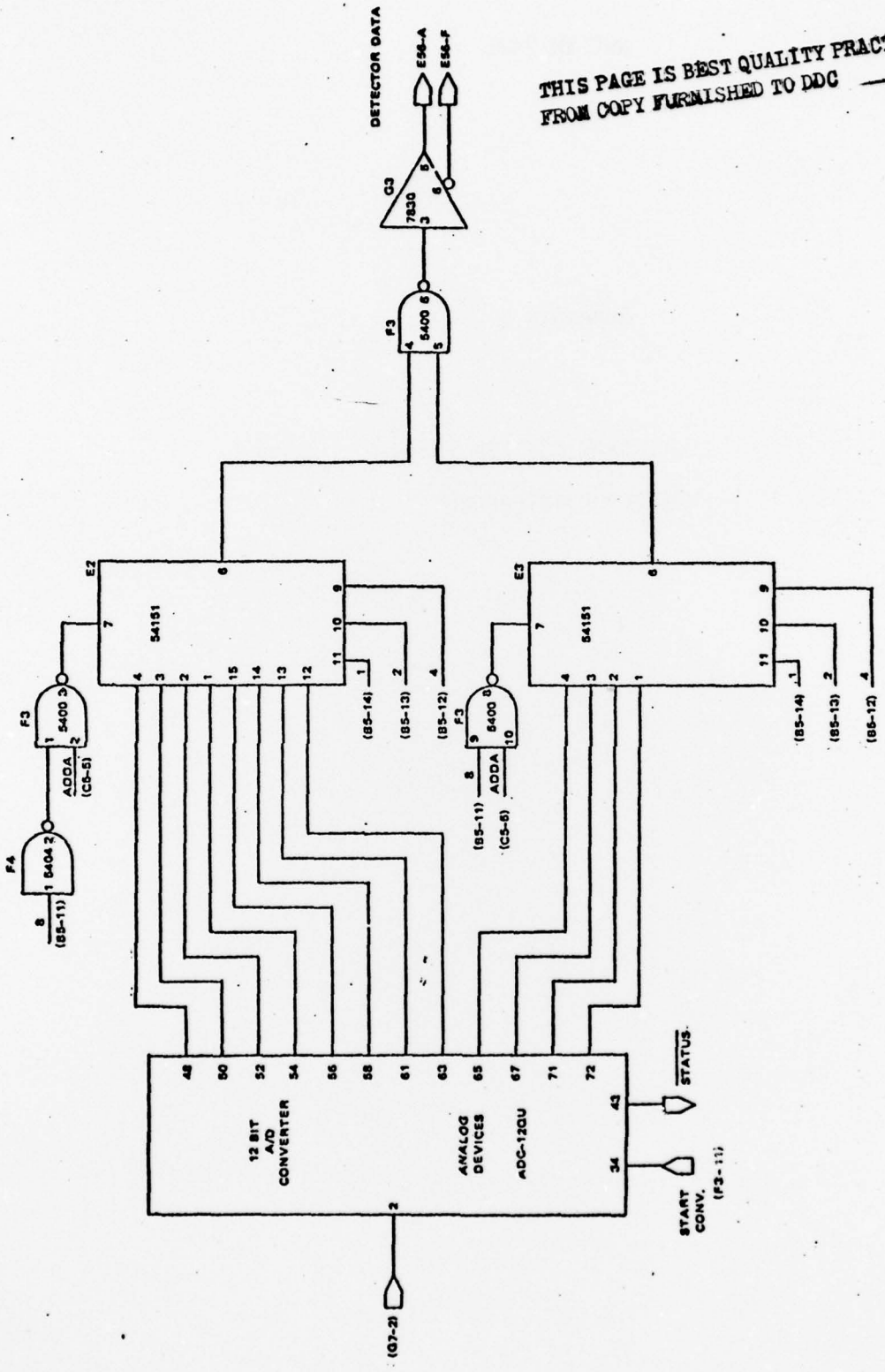
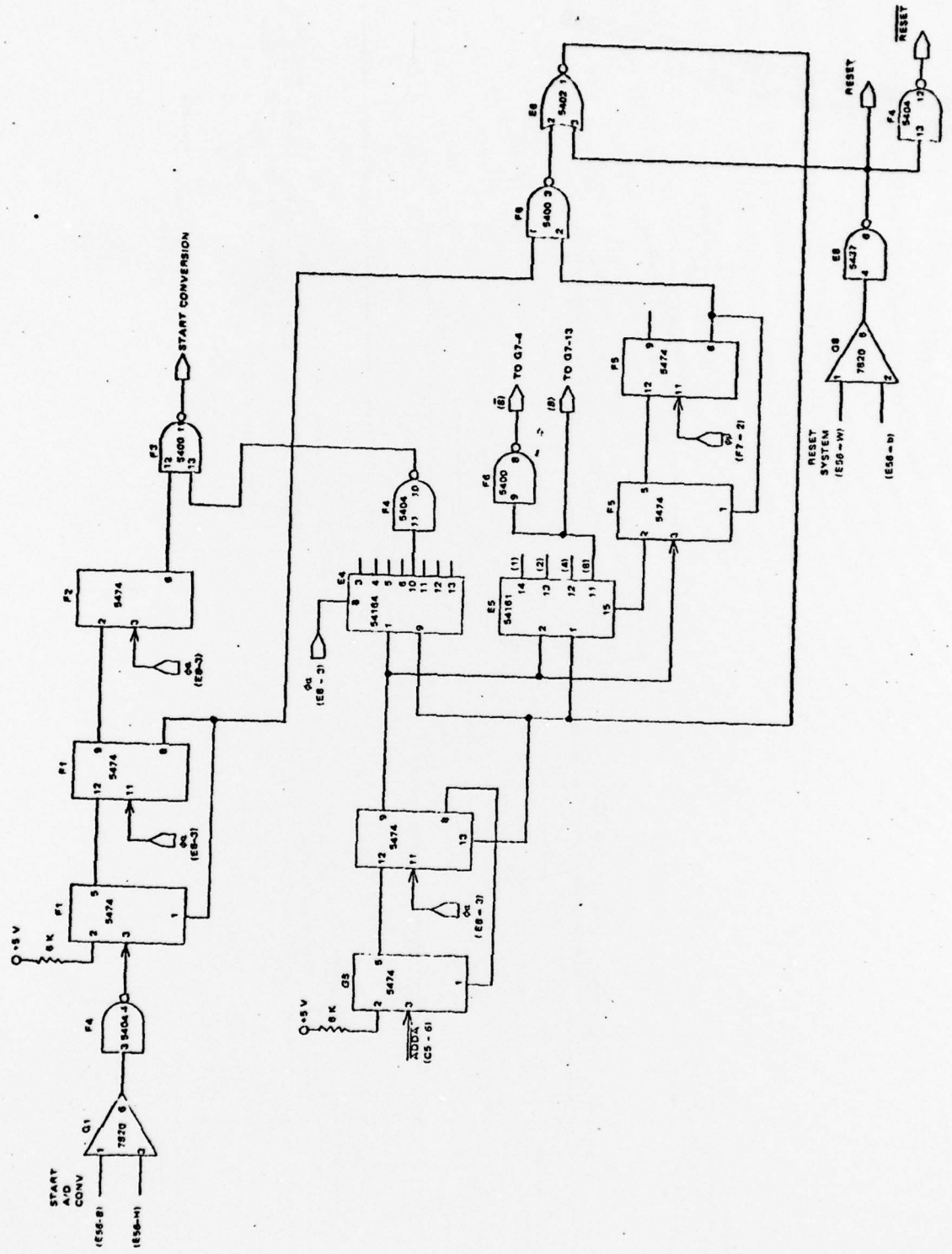
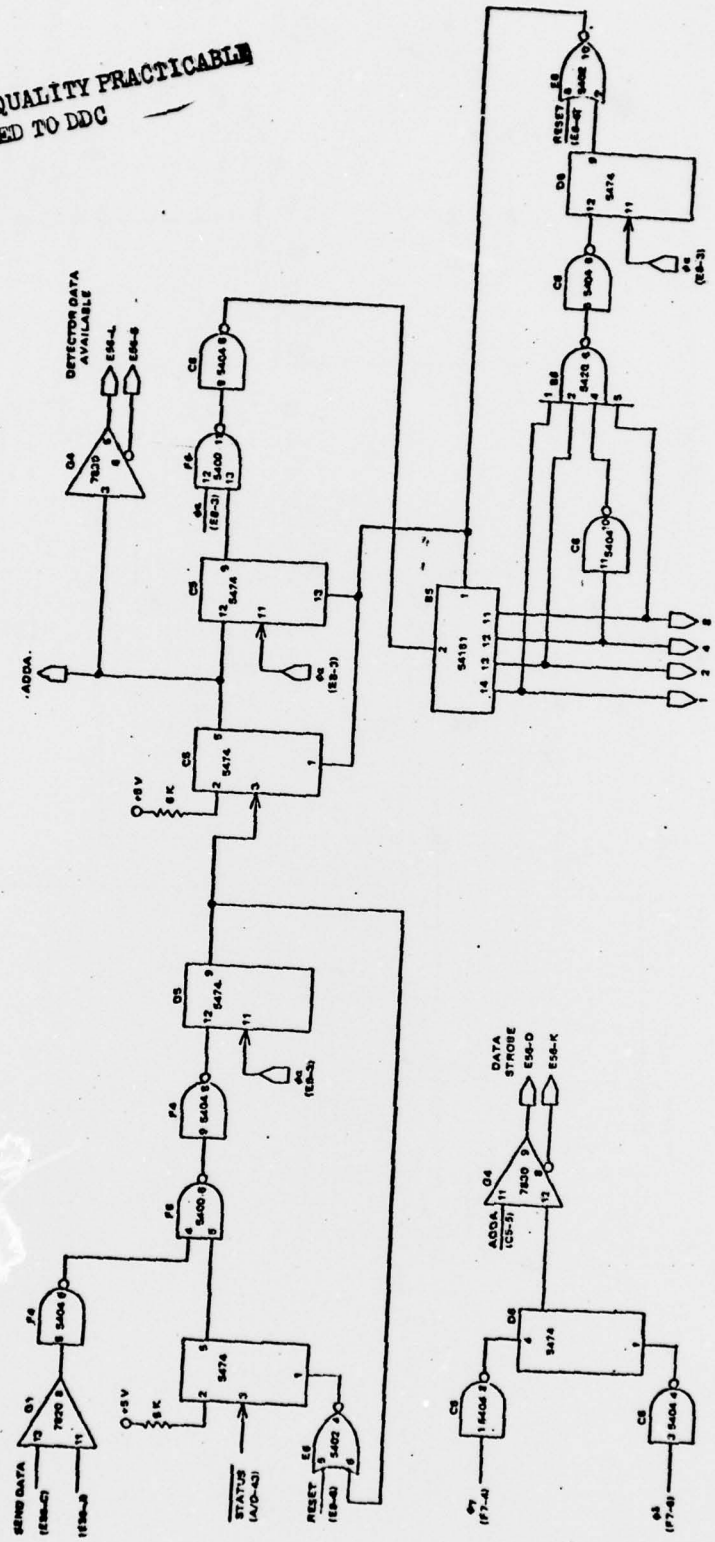
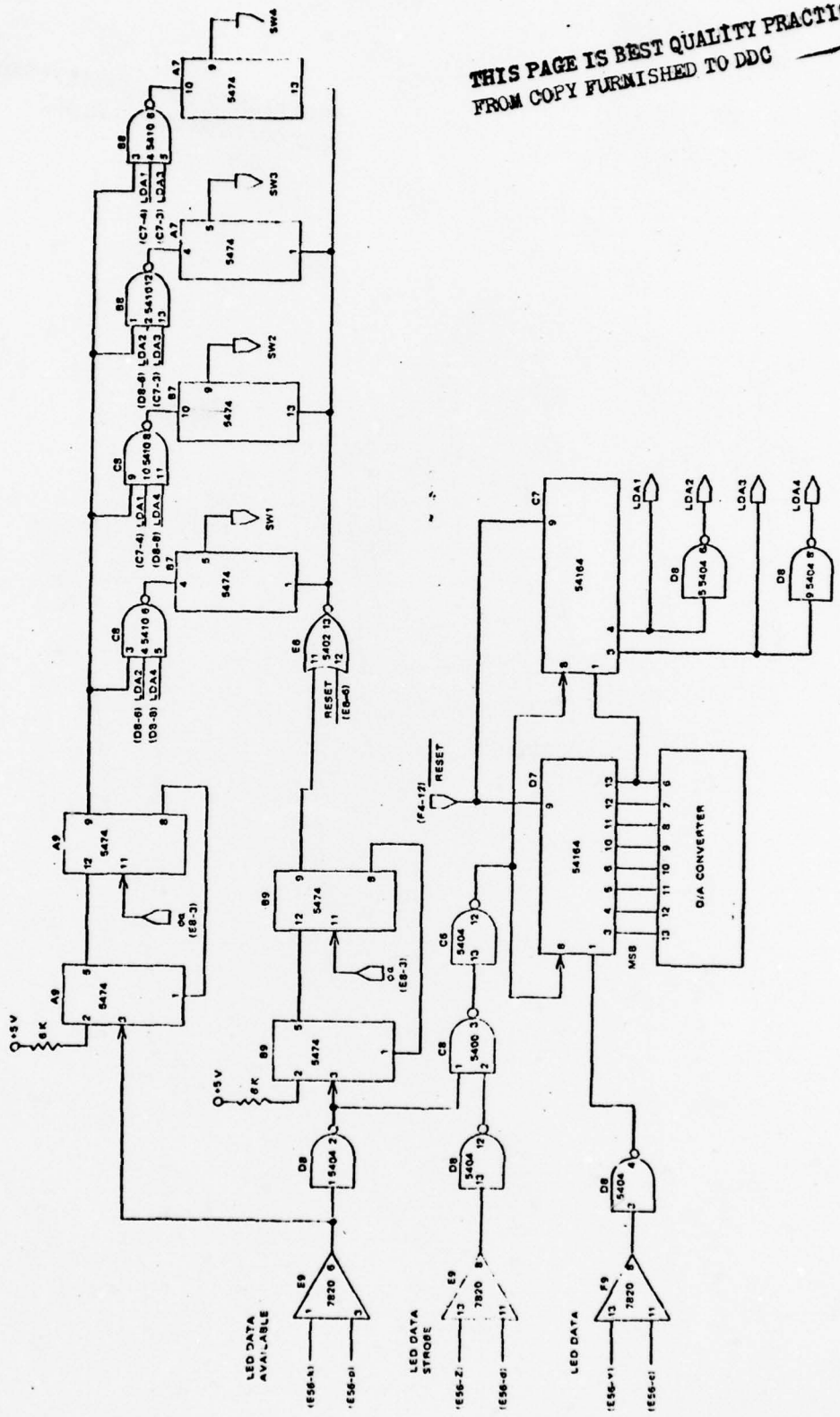
Appendix B

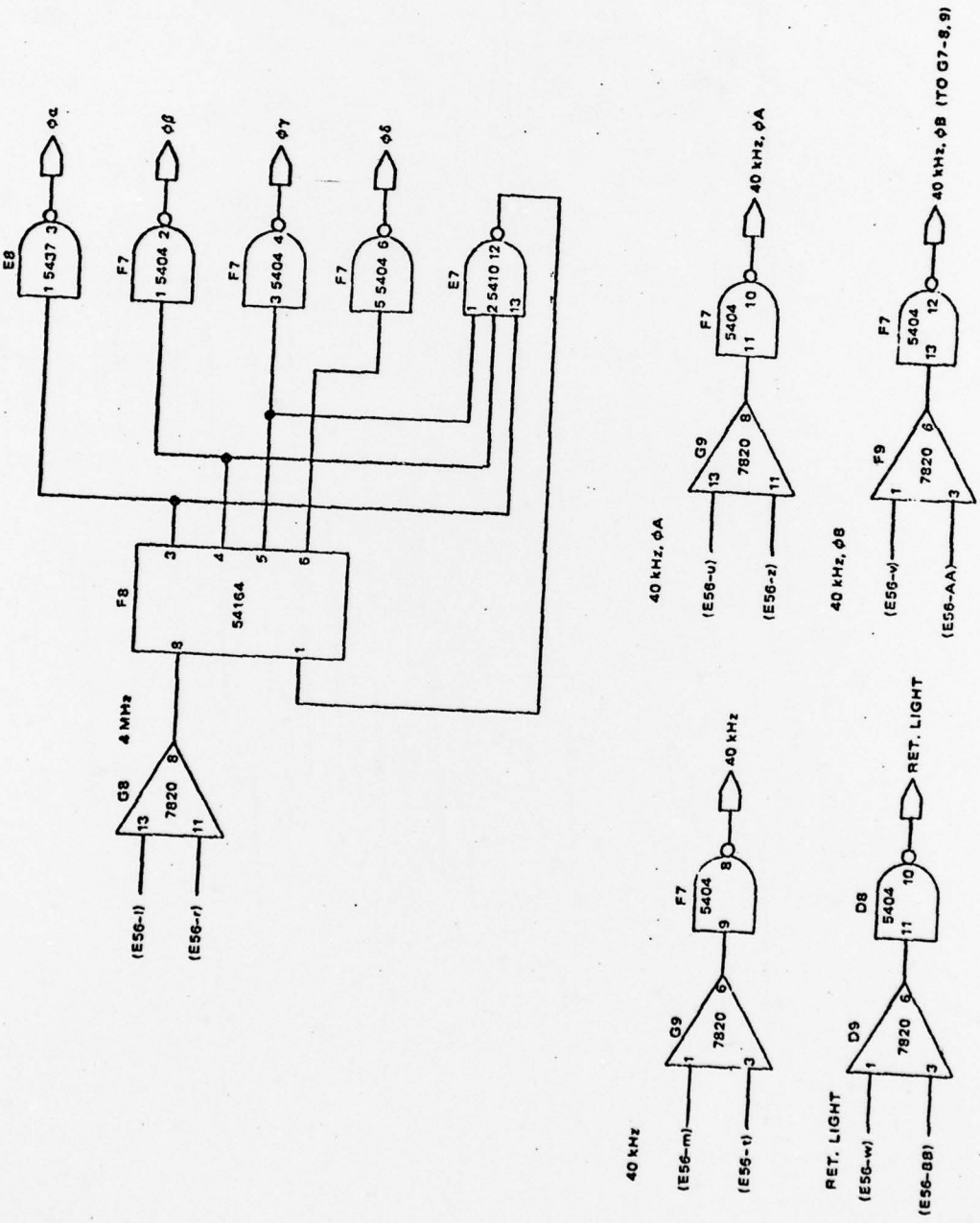
LOGIC DRAWINGS FOR THE DETECTOR INTERFACE





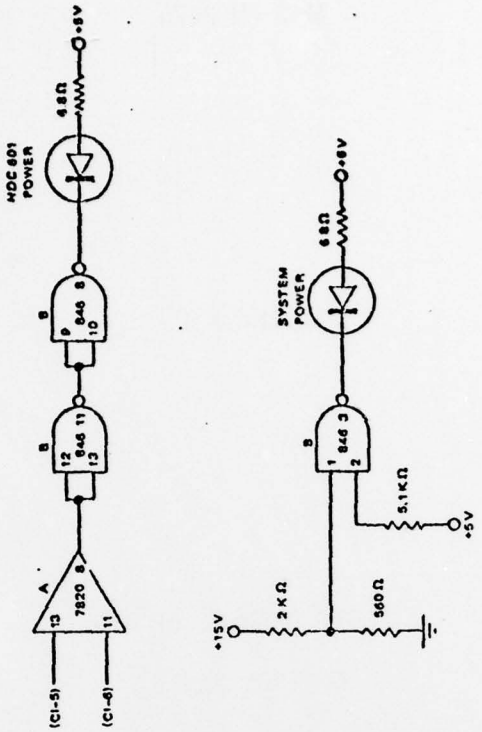


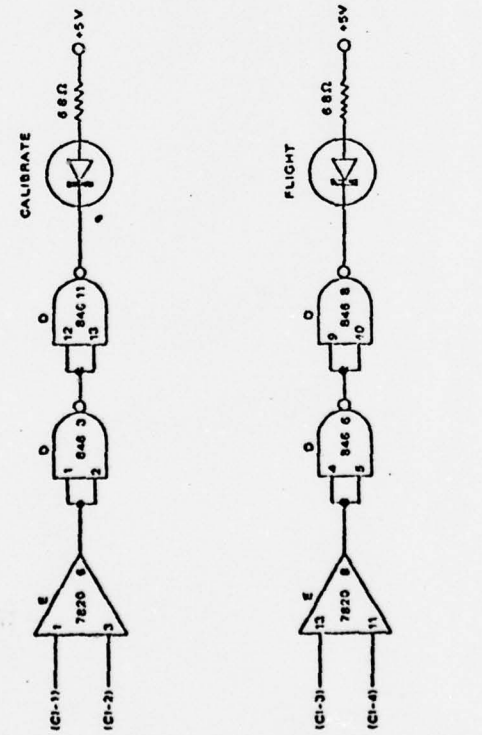




Appendix C

LOGIC DRAWING OF THE CONTROL PANEL


+5V
68Ω
HDC 601 POWER
846 8
846 11
7820
(C1-5)
(C1-6)
SYSTEM POWER
846 3
5.1KΩ
+15V
2KΩ
560Ω


CALIBRATE
FLIGHT
+5V
68Ω
846 11
846 3
846 8
846 6
7820
(C1-1)
(C1-2)
(C1-3)
(C1-4)